JUNE 2008

SEMI/Equipment Suppliers' Productivity Working Group 450 mm Economic Findings and Conclusions

INTRODUCTION

The history of the semiconductor industry is truly amazing. Over the life of the industry the cost per function has decreased exponentially, falling at a Compound Annual Declination Rate (CADR) of 29%. This has enabled semiconductor technology to penetrate mass consumer markets in addition to the defense and corporate IT environments that were its domain in the early years. Industry participants are rightly concerned that potential changes in this remarkable CADR might slow the growth of the market. While transistor scaling has been the key lever in cost reduction, other factors enter into the equation at varying levels of impact and investment. However, as the growth of the semiconductor industry has slowed and we reach the limits of device scaling, we must make difficult choices on where to invest the industry's increasingly scarce R&D funds. Assumptions and historical expectations must be challenged and replaced with objective analysis. This publication addresses the choices and challenges that the industry faces in this new business environment for funding optimal productivity improvements.

BACKGROUND

In November of 2005, the SEMI and SEMATECH Board of Directors members met to discuss two major concerns facing the semiconductor industry: an R&D funding gap and a significant deviation from the productivity improvements predicted by Moore's Law. The funding gap was described in a study SEMI had recently completed which showed that the equipment and materials industry was not generating enough revenue to fund the research and development needed to keep up with Moore's Law. The second challenge was the prediction by a subsidiary of SEMATECH, the International SEMATECH Manufacturing Initiative (ISMI), that the continued rate of decline in the cost of transistors was threatened. The boards decided to jointly form a study group to analyze the economics of the situation. The group, formed soon thereafter, was called the Joint Productivity Working Group, or JPWG. The suppliers' portion of the group was subsequently named the Equipment Productivity Working Group (EPWG).

Based on the charter to JPWG, EPWG has conducted simulation, survey, and modeling to support research, analysis, and discussion of the role of wafer scale-up in enabling continuous productivity gains. EPWG work over the past two years has shown that 450 mm wafer scale-up represents a low-return, high-risk investment opportunity for the entire semiconductor ecosystem; 450 mm should, therefore, be an extremely low priority area for industry investment.

INDUSTRY PRIORITIES

There Is No Imminent Productivity Crisis

Initial JPWG work has shown that ISMI's earlier assertion—that wafer processing cost curves were shifting unfavorably—was incorrect; no statistically significant shift in these costs is evident. The modeling of average processing cost history and

projections shows that the rate of reduction in cost per transistor can be maintained (within the analysis's margin of error) without a wafer scale-up.

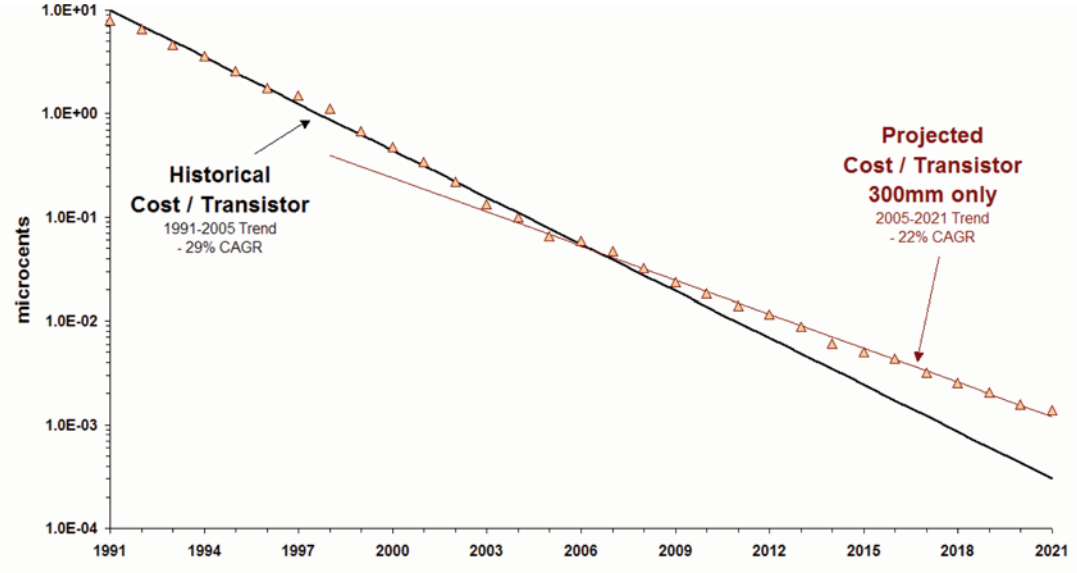
The original ISMI assertion of a change to a CADR of -22% popularized a few years ago (Figure 1) has been corrected; indeed, there is no near term point of inflection coming in the cost per transistor vs. time. Analysis of ISMI figures shows long term history of -29% CADR and near future of -28% (Figure 2). A 1% to 2% difference in slopes is statistically insignificant, as the standard deviation of the annual transistor cost trend is 12%; such a small difference in slopes is also insignificant when compared to the level of uncertainly in the thousands of assumptions built into the ISMI Economic Model.

If there is a slowdown in CADR, it would be the result of a lower growth rate for the industry as a whole, and, as a result, fewer available R&D resources. In order to extend the extraordinarily rapid rate of reduction in cost per transistor experienced during the late 1990's the industry would need to extend the booming market and economic conditions of the late 1990's, when rapid demand growth funding accelerated technology progress.

Limitations on R&D Resources Require Making Choices

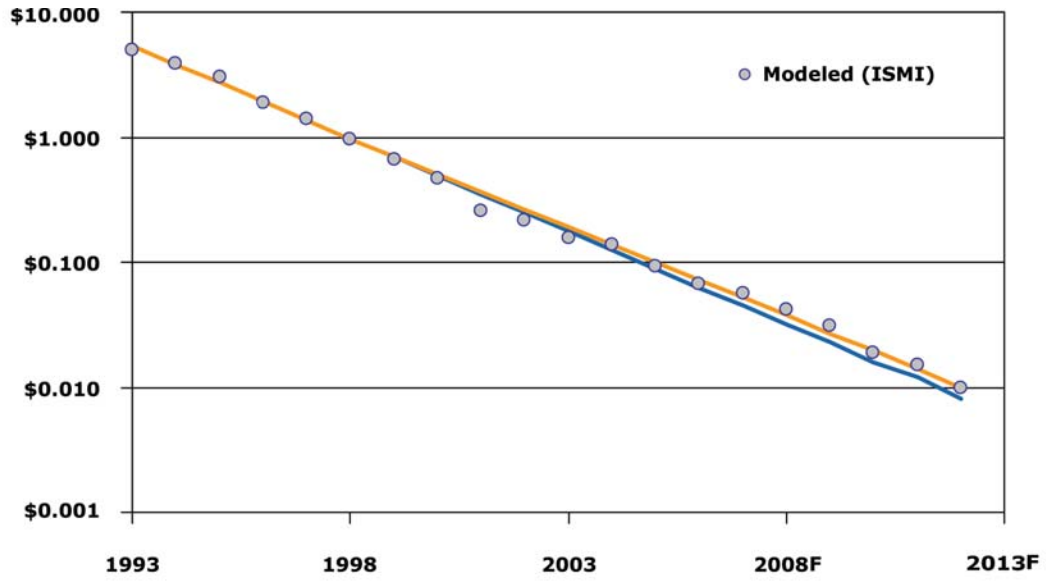
The equipment industry's R&D resources have become limited due to slower end-user demand growth, consumer-era economics, and the impact of the 300 mm transition.

Figure 1 **The "Productivity" Challenge—Average Fab Costs per Transistor**



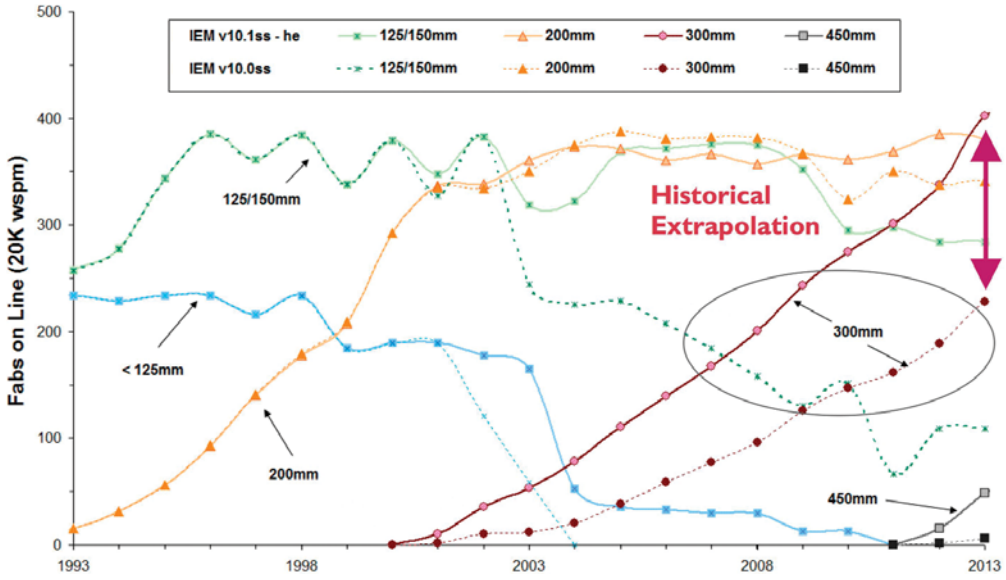
Source: ISMI

Figure 2 **The Challenge Revisited—Average Fab Costs (µ–¢/transistor)**



Source: Applied analysis of ISMI's Economic Model

Figure 3 **Growth Driving R&D Affordability**



174 Fewer Fabs:
Revenue loss to equipment industry: $261B

Available RD&E Funds:
Reduced by $30–35B

Source: ISMI analysis, JPWG, May 2006

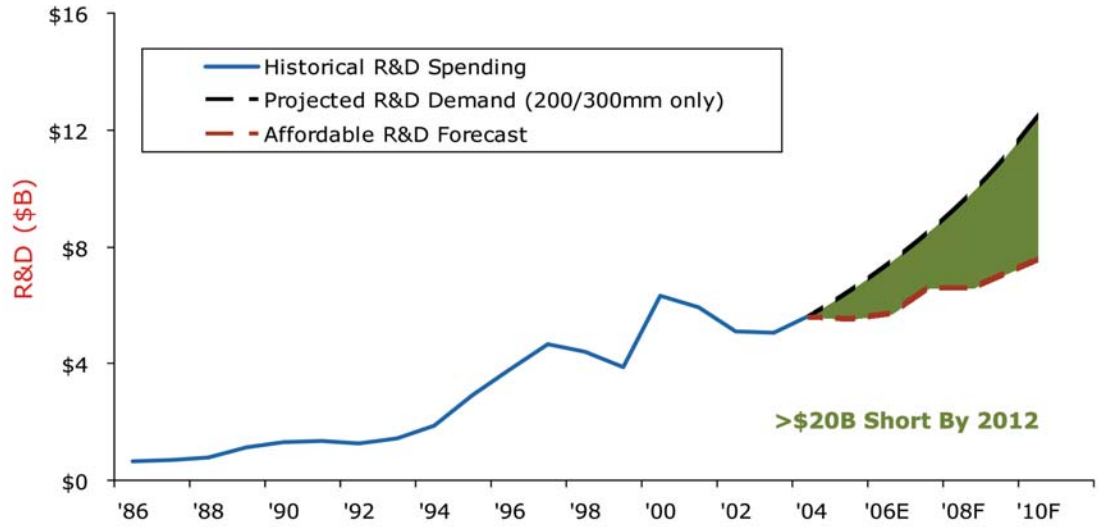
ISMI analysis has shown that actual build-up of 300 mm fabs has been well behind what historical extrapolation would suggest (Figure 3). By 2013, ISMI estimated, there will be 174 fewer 300 mm fabs than history would have suggested. EPWG calculated that those fewer fabs would amount to a cumulative loss of over a quarter of a trillion dollars in revenues to equipment suppliers; in turn, suppliers' ability to fund R&D would decline by $30 to $35 billion. This gap has been confirmed (albeit at a smaller level) by an independent SEMI study (Figure 4). As a frame of reference, the IC Manufacturers' R&D gap would be even bigger, as shown by ISMI (Figure 5, page 4).

Given the industry's limited R&D resources and the significant technical challenges ahead, it is important to follow careful ROI analysis and prioritization so as not to divert resources from the most critical programs.

Cycle Time Reduction Is Becoming a Priority

Modeling, surveys, and cross-industry discussions repeatedly highlight the increasing value placed on reducing cycle time through the fab. In this consumer-driven economy, demand is increasing for short life-cycle, smaller-run products, thus driving a high-mix production environment. Many chip designs' total production runs fit in one 300 mm FOUP, or even on as few as 5 to 10 wafers. Small-lot manufacturing is critical to allow a larger number of chip designs to efficiently use advanced technology—and it can also increase overall factory efficiency for large-lot fabs through faster cycle time.

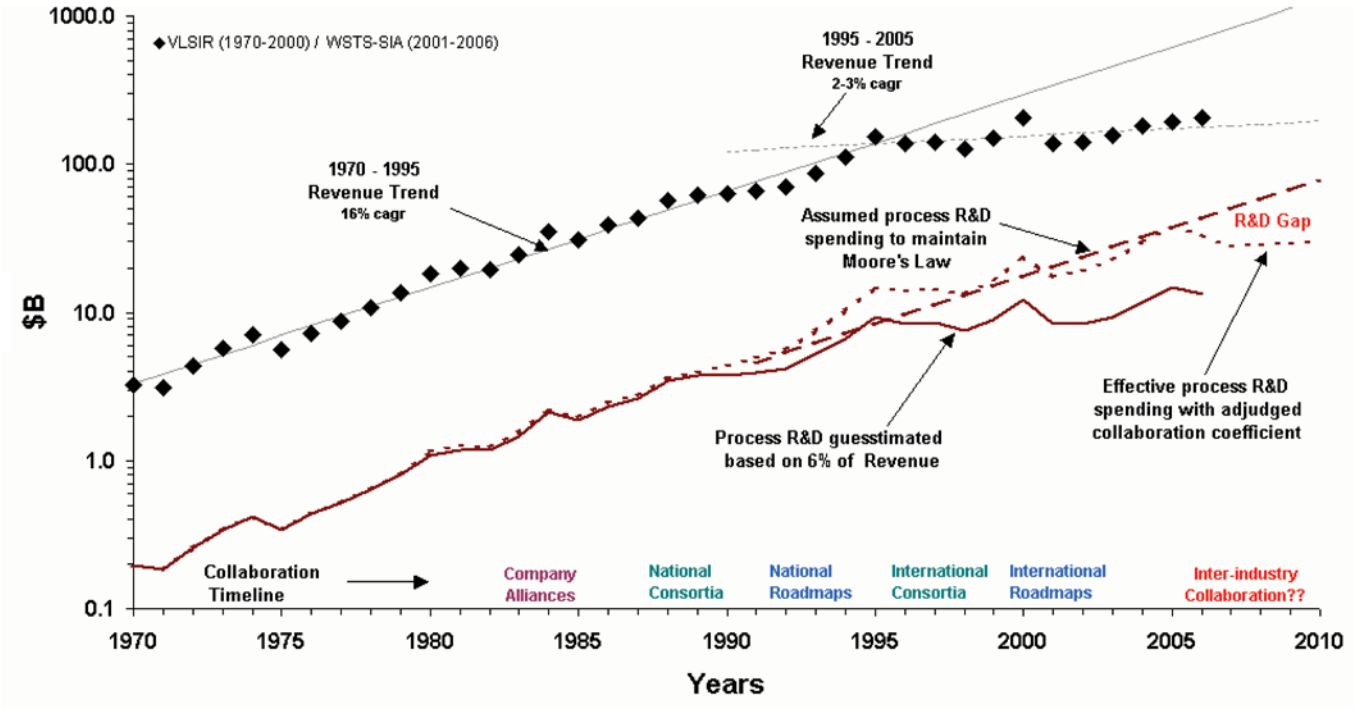
Figure 4 **R&D Investment Gap in the Equipment Industry**



Note: Affordable R/D forecast assumes 14% of equipment industry revenues

Sources: S&P, SIA, SEMI, Infrastructure Advisors

Figure 5 **R&D Investment Gap in the Semiconductor Industry**



Source: ISMI

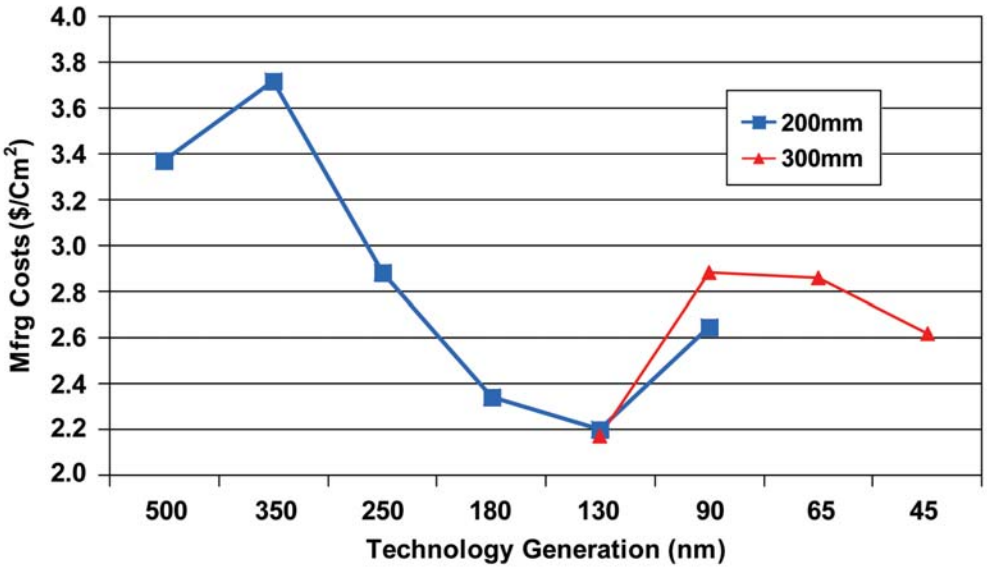
THE ECONOMICS OF WAFER SCALE-UP: FACTS VS. FOLKLORE

Wafer Scale-Ups Do Not Provide Their Assumed Economic Benefits

A conventional industry assumption is that larger wafers lead to lower production costs, and are required to maintain industry economics. However a detailed "apples-to-apples" analysis of ISMI's economic model reveals a different conclusion: the 300 mm generation has increased processing costs relative to comparable 200 mm technology (Figure 6).

The scale-up to 300 mm wafers did not significantly reduce the net manufacturing costs for the industry as a whole, and definitely not anywhere near its touted "savings" of 30%.

Figure 6 **Economic Impact of Wafer Size Transition—Manufacturing Cost Trend**

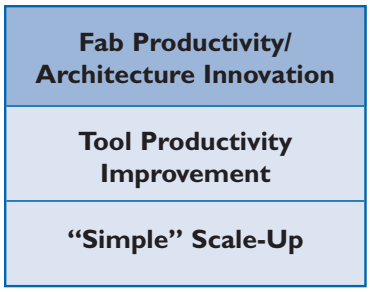


Note: Year 3 of production, Leading Edge Memory

Source: Applied analysis of ISMI's Economic Model

Figure 7 What DOES a Scale-Up Do for Fab Productivity?

Key drivers of historical apparent benefits of wafer scale-up—fab innovation and fab productivity gains—can and should be independently pursued in the 300mm tool set.



Specifically, had the industry continued to invest in improving the technical and operational performance of the 200 mm tool set, its cost structure may have continued to be comparable (or perhaps even superior) to 300 mm; however, the industry had to cut the 200 mm investment due to R&D constraints mentioned above, thereby giving rise to what was an apparent advantage of 300 mm.

There is thus no foundation for the assertion that the semiconductor industry "needs 30% wafer cost reduction through a wafer size transition every 10 years," as the 300 mm scale-up by itself has not provided such benefits.

It is important to note that a wafer scale-up typically involved a number of high-return automation and architecture shifts and tool innovations, combined with what is a low-return raw wafer diameter increase (Figure 7). While these shifts have historically coincided, architectural innovation is not inherently dependent on wafer scale-ups. Key drivers of historical apparent benefits of wafer scale-up—fab innovation and tool productivity gains—can be independently pursued in the existing tool set. Therefore, EPWG's analysis has focused on analyzing the "simple scale-up" scenario: the cost/benefit effect of increasing the diameter of the wafers through the fab, excluding the effects of any coincident innovation in fab architecture or tool design as these innovations could have been applied to the current tool set.

True Incremental Costs of Wafer Scale-Ups Overwhelm Their Benefits

A review of intrinsic savings demonstrates that the net benefits of scale-up represent at most a few percentage points of fab processing costs.

Studying the experience of the 300 mm transition was instrumental in understanding the cost/benefit equation of scale-ups. The supposed 300 mm "savings" were really due to

- Counting the favorable effects of initiatives which were not specific to wafer scale-up (such as factory automation/AMHS introduction, tool throughput improvements, Advanced Process and Equipment Control, FOUP introduction, etc.)
- Stopping work on earlier 200 mm tool set
- Ignoring cross-industry costs (to suppliers and non-users)
- Disregarding the upfront investment

Such analysis entails careful modeling. It is not accurate to simply assume that scale-ups enable broad cuts in spending in most fab processing costs (Figure 8). In reality, fab costs consist of a complex portfolio of costs, some of which are unfavorable to wafer scale-up (such as substrate costs), some of which are neutral (such as many of the processing and metrology tools and most of consumable costs), and some of which may be favorable.

Within cost components, it is important to consider the intrinsic impact to costs: for example, how much more expensive would it be to build equipment to handle larger wafers, as opposed to whatever price that equipment may fetch. For example, Equipment costs increase significantly in a scale-up, partly due to the costs of assembling larger, heavier, higher-tolerance machines and partly due to the opportunity cost of lost economic advantage (transition to new, higher-capacity machines significantly undermines cost and reliability benefits realized thanks to learning and volume economics).

The EPWG built its analytical toolkit to determine the specific benefits of scale-up and its total cost impact to the industry. One key element in the EPWG toolkit developed was the Cost/Benefit Model (CBM), which seeks to provide a transparent, clear and simple analysis of the overall cost/benefit

Figure 8 ISMI 450mm Transition Assumptions (32 nm, 2012, Foundry)

Cost Components	Share of Fab Costs	Cost Multiple	Output Multiple	Spend Impact
Fab Capital Spend	50%	1.3	2.3	-45%
Utilities & Maintenance	19%	1.3	2.3	-45%
Substrate	7%	5.5	2.3	135%
Other (Labor, Materials)	24%	1.3	2.3	-45%
Total (Wafer Costs)	100%	1.6	2.3	-32%

Source: Analysis of ISMI economic projections

of a wafer scale-up (although the model can be applied to any proposed improvement in fab throughput). The CBM is based on viewing the entire industry as one economic entity. As a result, the analysis associates benefits with all of the costs required to generate them. The CBM considers the universal impact of initiatives; for example, it actually eliminates the effect of "savings" which accrue to users of scaled-up fabs but which effectively are cost transfers (due to losses and opportunity costs incurred by suppliers, third parties, and non-users of the larger fabs); as a result, the industry-wide net benefits are much smaller.

Even if Scale-Ups Provided Solid Net Benefits, Those Would Not Suffice to Recoup Investment

Wafer size scale-up represents the single largest and most disruptive type of investment which the industry could undertake. Every piece of process and automation equipment must be redesigned and integrated, using a large number of extremely expensive test wafers (at 9 to 14 times the cost of existing production wafers). In addition, the high level of uncertainty in timing (to get to "complete industry readiness") raises the likelihood of delays and shifts in the adoption schedule, further increasing required investment.

This scenario played out during the 300 mm transition, when a pull from early adopters and subsequent changes in priorities and schedules resulted in uncertainty, redundancy, and waste, thus inflating RD&E investment (primarily borne by suppliers).

SEMATECH has estimated the costs of the 300 mm wafer size transition at $25–30B. A financial analysis of the R&D spending patterns across the semiconductor ecosystem over the past decade supports this estimate and suggests a total cost for the transition of over $22B (Figure 9).

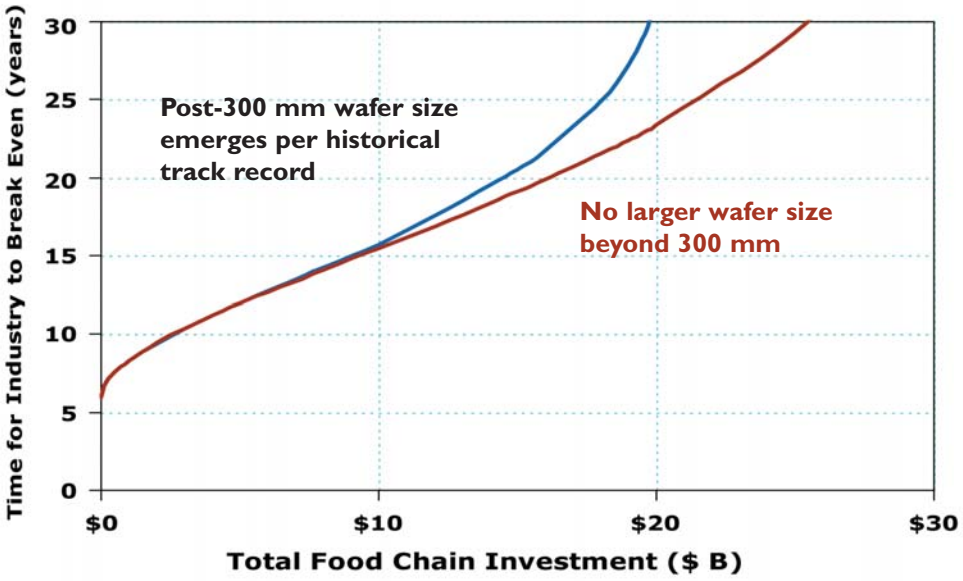
The industry as a whole may never recoup this investment. Even if the industry realized 30% savings on every 300 mm wafer produced (an assumption which is clearly overly

Figure 9 **Investment in 300 mm Transition**

$M	SEMI Manufacturers	Equipment Suppliers	Equipment/Semi Ratio	Excess Investment
CY87	$2,299	$1,265	55%	
CY88	$2,549	$1,492	59%	
CY89	$2,810	$1,149	41%	
CY90	$2,918	$1,362	47%	
CY91	$3,019	$1,698	56%	
CY92	$3,112	$1,602	51%	
CY93	$3,275	$1,951	60%	
CY94	$3,623	$2,629	73%	
CY95	$4,545	$3,783	83%	$1,168
CY96	$4,537	$4,726	104%	$2,115
CY97	$5,173	$5,546	107%	$2,569
CY98	$5,109	$4,877	95%	$1,937
CY99	$6,023	$5,221	87%	$1,755
CY00	$7,560	$7,582	100%	$3,232
CY01	$7,163	$7,341	102%	$3,219
CY02	$7,808	$6,055	78%	$1,562
CY03	$8,493	$5,635	66%	
CY04	$9,830	$6,432	65%	
CY05	$10,416	$6,505	62%	
CY06	$12,448	$6,888	55%	
				$17,556
Average 1995–2002			95%	
Other Years			58%	
Manufacturer Investment (5–10% during period)				**$2.3–4.5B**
Sub-Supplier Investment (10% of supplier)				**$1.8B**
Total				**$22–24B**

Note: Does not reflect change in investment mix, e.g., suppliers reprioritizing new markets over WFE

Figure 10 **300 mm Investment May NEVER Be Repaid—Recouping the Industry's 300mm Investment**



Assumptions: Semiconductor industry trending from about $200B at 8% p.a.; semiconductor companies enjoy 45% gross margin; 55% of semiconductor costs are in wafer fabrication; 30% of die costs can be reduced via 300mm adoption; initial investment is distributed evenly over a six-year period; cost of capital is 20%; for baseline (implicitly assuming larger wafer generations)—300 mm follows a 30-year life cycle, peaking at 50% of silicon area processed; for alternative scenario: 300 reaches 100% of silicon area processed.

optimistic, as mentioned above), it would take 30 years or more for the entire industry to reach payback (Figure 10). If savings are indeed much smaller, 300 mm investment may never be fully paid back, as the effective life of wafer diameter generations has historically been less than 30 years.

450 MM: A PARTICULARLY WEAK CASE

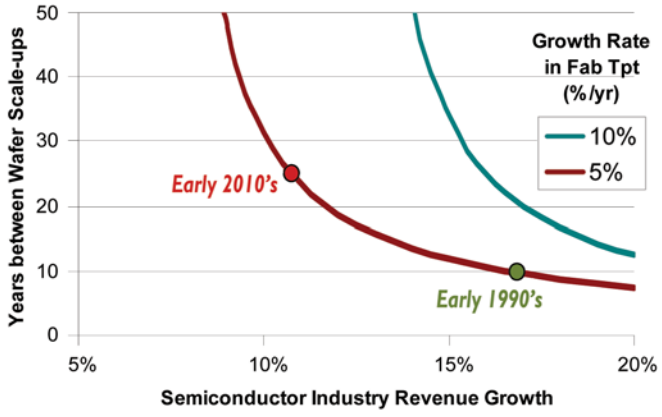
With Slower Demand Growth, Scale-Up Will Not Be Needed for a Very Long Time

The traditional motivations for wafer scale-ups—a rapid growth in silicon area processed (requiring very rapid increase in the number of fabs) or a secular increase in die size (driving unacceptably low yields in existing wafer sizes)—are not evident as the industry considers a possible transition to 450 mm.

Historically, with rapid industry growth, the impetus to control the number of fabs was an important concern in timing wafer transitions. But with slower demand growth, scale-up would not be needed (from a "number of fabs" perspective) for a very long time: timing between wafer diameter generations can increase from ~10 years (historically) to ~25 year cycle without causing a disturbing increase in fab count (Figure 11). If this were the only consideration in the analysis, this would suggest a possible 450 mm transition by about 2025. It is quite evident that significant wafer size scale-ups have become less frequent over the years, and extrapolating those trends suggests that no size transition may ever be required (Figure 12, page 8).

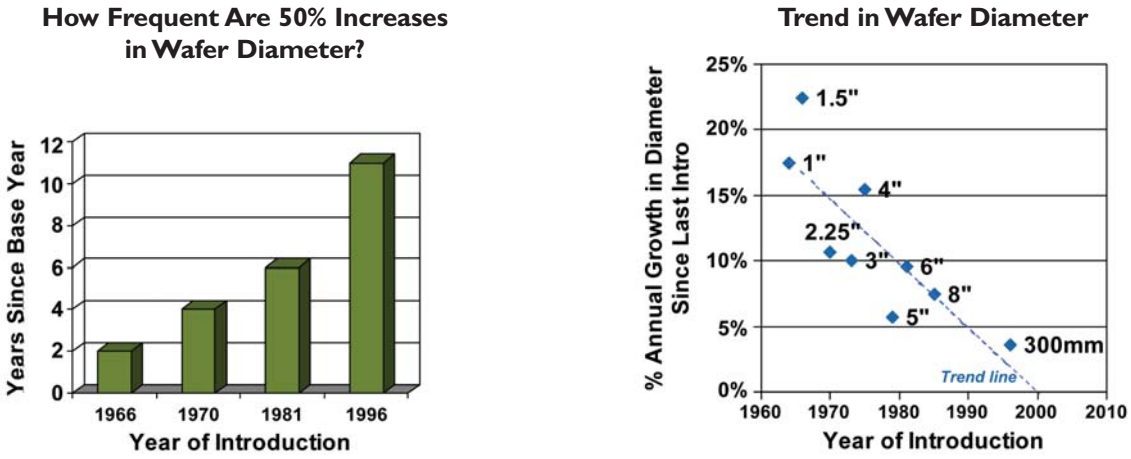
It is also important to bear in mind that the 300 mm transition was the largest relative scale-up ever introduced, and it coincided with the most significant industry slow-down; this would ostensibly provide the industry with enough available scale increase for a long period (Figure 13, page 8).

Figure 11 Seeking to Limit Number of Fabs… Then and Now—Demand-Driven Need for Scale-Up?



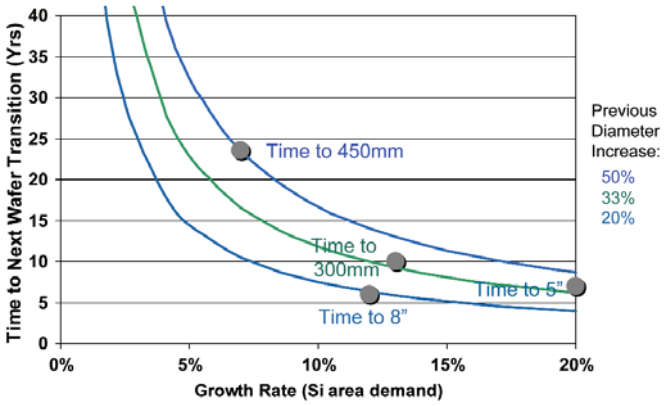
Assuming 2% annual inflation in price per Cm^2

Figure 12 **The "Productivity" Challenge**



Source: IC Knowledge

Figure 13 **Drivers of Wafer Diameter Increase**



Note: Model assumes/implies that (1) cost savings are proportional to scale-up, (2) savings dissipate as a function of business growth, and (3) next wafer introduced when all savings from its predecessor have dissipated.

At the same time, with chip architecture innovation, new packaging, and projected demand mix, there are no near-term concerns about the impact of increasing die size as a key driver for larger wafers.

Recent Shifts in Fab's Cost Structure Make Scale-Up Less Attractive

Based on bottom-up analyses of fab economics and operations, EPWG has shown that the economic benefits of a wafer scale-up are intrinsically limited, and in fact are shrinking.

One cannot assume that a wafer scale-up would enable all tools to become twice as productive as existing tools (Figure 14). The basic limits of physics dictate that process tools which have a throughput based upon area scan rates could enhance their throughput during a 450 mm transition by an output multiplier averaging only 1.24 (Figure 15). This would mean that a 450 mm fab would need almost twice as many beam tools to process the same number of wafers as an existing 300 mm fab.

Figure 14 **ISMI 450 mm Transition Assumptions (32 nm, 2012, Foundry)**

Cost Components	Cost Multiple	Output Multiple	Net Spend Impact
Plasma Tools	1.23	2.31	-47%
Beam Tools	1.30	2.31	-44%

Source: Analysis of ISMI economic projections

Figure 15 **Beam Tools Analysis**

	Share of "Beam" Spend	Output Multiplier
Litho	70%–75%	1.18
Metrology & Inspection	22%–24%	1.40
Implant	3%–6%	1.39
Average "Beam"	—	1.24

When combined with the cost increase of such larger systems (Figure 16, page 9), it can be shown that these tools actually become 5% less productive (Figure 17, page 9). Other elements of fab costs—such as consumables—are similarly neutral or slightly unfavorable to scale-ups.

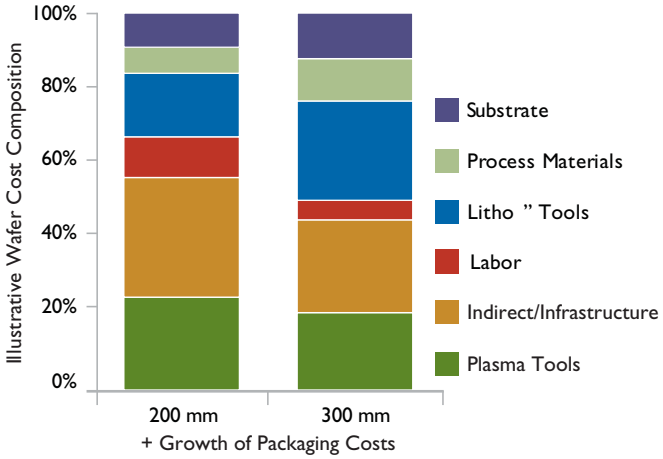
In fact, the fab cost structure has become more area-driven, or less favorable to a scale-up (Figure 18, page 9), due to the relative increase in the share of lithography, metrology, materials, and substrate within the overall cost. Furthermore, in many cases fab costs represent a smaller share of total final product cost than has been seen historically, due to the increasing spending in yield, assembly, packaging and test. As a result, a transition to 450 mm would certainly not be key to economic benefits.

Figure 16 Beam Tools Cost

Materials Quality/Resizing	+15% to +25%
Volume Reduction	+3% to +5%
Loss of Learning	+5% to +10%
Combined Impact	**+20% to +40%**
ISMI Assumption	**+30%**

Note: "Materials Quality/Resizing" figures are merely an illustration, rather than the result of detailed bottoms-up analysis

Figure 18 Wafer Costs— Scale-Up Benefits Shrinking



"Expected" 450 mm Benefits Run Counter to Fact and Analysis

An industry-wide analysis shows that a move to 450 mm wafers is likely to be no more productive, and very likely even less productive than continued focus on 300 mm, in terms of cost per transistor.

An accurate model of a 450 mm fab using the proper number of lithography, ion implant and metrology tools needed to match the wafer output of a 300 mm fab would show a significant increase in the required capital spending.

The only way to realize the cut of 45% in fab capital spending (needed to reach the industry hope for a 30% productivity improvement) would be a 30% to 60% cut in equipment costs below even the 300 mm baseline (Figure 19)— an entirely impossible conclusion, given the higher costs of 450 mm equipment. The 450 mm fab model must also address the similar concerns regarding the total cost of process materials, whose use is largely driven by area-dependent processes.

It is clear that realizing the 30 percent savings "expectation" by implementing 450 mm is a mathematical impossibility (Figure 20, page 10) even before taking into account the increased R&D investments.

Figure 17 Implications for ISMI 450 mm Transition Assumptions (32 nm, 2012, Foundry)

Cost Components	Cost Multiple	Output Multiple	Net Spend Impact
Plasma Tools	1.23	2.31	-47%
Beam Tools	1.30	~~2.31~~ 1.24	~~-44%~~ +5%

Source: Analysis of ISMI economic projections

Fact-based analysis of output multiples highlights a critical flaw in "Blue Diamond" analysis: No justification for desired reduction in net spend.

Figure 19 Other ISMI 450 mm Transition Scenarios

Option A: Cost Components	Cost Multiple	Output Multiple	Net Spend Impact
Plasma Tools	1.23	2.31	-47%
Beam Tools	~~1.30~~ 0.70	~~2.31~~ 1.24	-44%

Option B: Cost Components	Cost Multiple	Output Multiple	Net Spend Impact
Plasma Tools	~~1.23~~ 0.39	2.31	~~-47%~~ -83%
Beam Tools	1.30	~~2.31~~ 1.24	~~-44%~~ +5%

Source: Analysis of ISMI economic projections

Alternative scenarios are equally impossible, highlighting a critical flaw in "Blue Diamond" analysis: No justification for desired reduction in net spend.

EPWG has sought to shift from intuitive consensus over "expectations" to logical modeling in analyzing 450 mm. The cost/benefit model (CBM) has been used to analyze the transition by considering different intrinsic costs (which respond differently to distinct physical or economic shifts) including the operational penalties (in terms of Overall Equipment Efficiency, or OEE) associated with a "simple scale-up." The conclusions are quite clear (Figure 21, page 10): 450 mm will not provide any cost savings. From the perspective of the entire industry, intrinsic die cost could increase by up to 25 percent with migration to 450 mm over a lifetime of 20 years or more (if the technical challenges of substrate production and equipment scaling are successfully solved); the economic penalty for the industry would be much larger during the earlier years of penetration. Any savings realized by specific device manufacturers would come at the expense of the majority of the industry and its ecosystem.

Figure 20 **Interim Summary (ISMI Cost Basis)**

Cost Category	Beam Tools	Substrate (incl. monitors)	Consumables	Other	Total
300 mm Baseline					
Percent of CoO	15%	15%	27%	43%	
CoO	$920	$878	$1,619	$2,628	**$6,045**
Impact of Next Wafer Size					
Relative Cost Impact	5%	135%	-1.9%		
Impact of Equivalent CoO	$46	$1,185	(30)		$1,201
Expected Cost Savings	30%				$(1,814)
Expected CoO per eq. Wafer	30%				$4,232
Cost Reduction Required to Meet Expectation				$(3,015)	
Cost Reduction as Percent of Category				**-115%**	

Figure 21 **Scale-Up Impact on Costs**

Lifetime Cost Category	Driven Processing (CapEx)	Area-Driven Processing (CapEx)	Other Capex	Substrate	Wafer-Driven Operating Expense	Area-Driven Operating Expense	Other Expense	Total
Examples	Vacuum Tools	Litho, Implant, M&I	Atmospheric Tools		Labor	Materials	Infra-Structure, Maintenance	
300 mm Baseline								
Percent of CoO	15%	21%	6%	12%	18%	8%	20%	$2,140
Average Gross Margin %	45%	45%	45%	30%	0%	30%	0%	
CoO (Intrinsic Cost)	$173	$253	$71	$177	$383	$121	$427	$1,605
Impact of Next Wafer Size								
TPT Impact (area per hour)	131%	24%	131%	131%	131%	131%	131%	
Intrinsic Cost Impact								
Physical Scaling	97%	40%	69%	549%	13%	108%	69%	
Reduced Volume	7%	3%	6%	0%	7%	7%		
Lost Learning	18%	18%	18%	43%	3%	3%		
CoO (intrinsic) per 300 mm Wafer	$186	$346	$65	$713	$206	$121	$311	$1,949
OEE	33%		32%					
Adjusted CoO (intrinsic) per 300 mm Wafer	$192	$357	$67	$735	$213	$124	$321	$2,010
Net Savings per Wafer	**$(404)**	**25%**						

per ISMI | per SEMI model | due to granularity, set-up | per SEMI bottom-up analysis | average

450 MM: UNATTRACTIVE RISK/RETURN PROFILE

Questionable 450 mm Benefits Cannot Justify the Required Investment

The small to negative savings offered by 450 mm are insufficient to recoup the huge investment in the transition.

Even if 450 mm did provide net cost savings, the industry would be unlikely to recoup its 450 mm investment (which is likely to run $20B or more for the entire food chain, if similar to the 300 mm transition). Earning a 15% to 20% ROI would require the construction of four to eight 450 mm fabs per year every year over at least 15 years for the semiconductor ecosystem to pay back the development costs—even with optimistic cost savings (Figure 22). Such a massive building boom is highly unlikely to happen in the best of cases.

More generally, the rate of net savings and industry adoption/penetration ultimately combine to put a hard limit on economically-affordable investment across the industry for any new initiative (Figure 23). It is clear to see that 450 mm combines low (to no) net savings, limited potential penetration, and exceedingly high investment; it thus constitutes a highly improbable candidate for rational allocation of investment capital.

450 mm Offers Little—If Any—Upside Opportunities

Adopting 450 mm (despite all the above reservations) will not trigger faster industry growth sufficient to compensate for the negative impact to the supplier base. Potential impact on end-user demand growth would not suffice to countervail the negative impact of reduced growth and profitability.

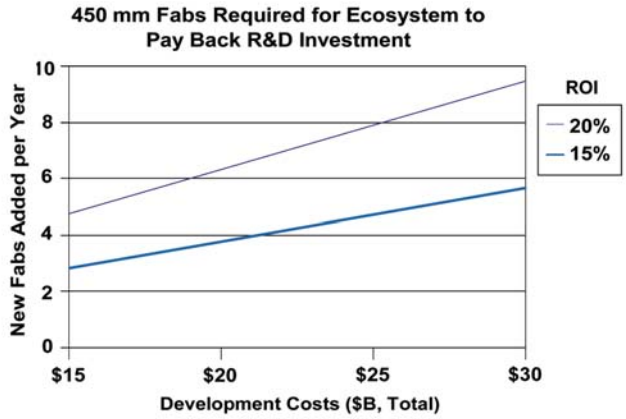
Scale-up is unlikely to generate any noticeable positive effect on price/function. The basic cost of wafer processing represents about 15% of price/function for advanced MPU (Figure 24, page 12), and even less for an ASIC produced by a foundry (Figure 25, page 12). Even if it were possible to realize the 30% reduction in fab costs, the effect on the price of the finished device would be less than 10%.

As a result, the industry cannot generate enough incremental revenues to justify the costs of a transition to 450 mm wafers. For example, even if one accepts the simple conventional "expectation" of 30% savings due to 450 mm and assuming an elastic market demand , net benefit to manufacturers would be under $30B over 15 years, in present value, but the net loss in present value to the supplier industry could exceed $200B (Figure 26, page 12). Clearly the loss to suppliers is several times larger than the benefits to customers.

450 mm Introduces Significant Downside Risks

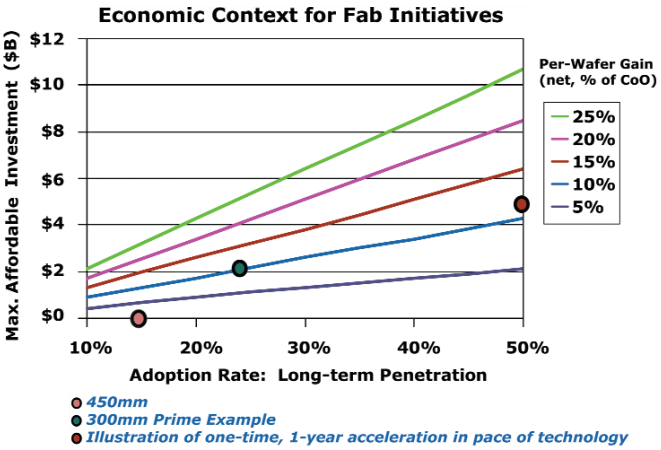
As noted before, a wafer scale-up is likely the riskiest investment which the industry could undertake. In addition to high direct costs and upfront investments, manufacturers will also incur significant cumulative loss of yield and productivity—which, in the cases of unforeseen delays, would become severe.

Figure 22 Only Robust, Broad-Based Adoption Can Justify 450mm Investment



Assuming 20% savings due to scale-up

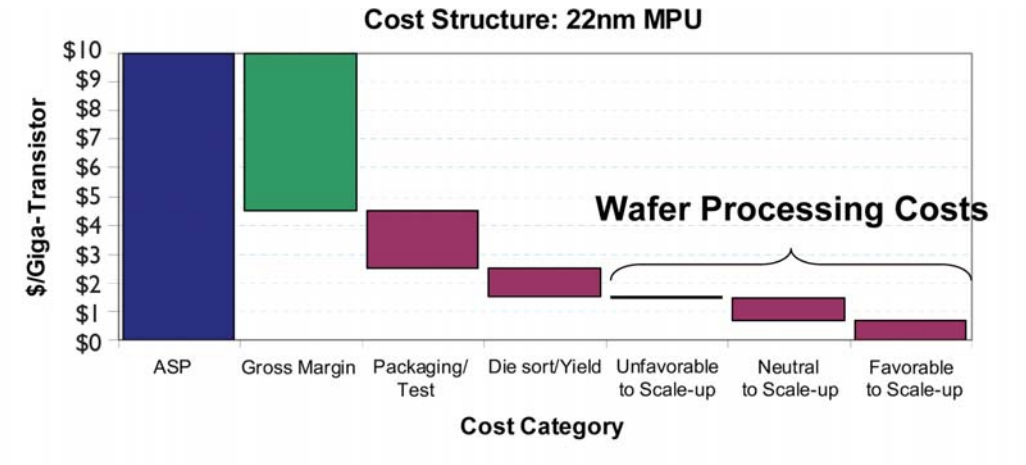
Figure 23 Screening Tool



Business risk and uncertainty are paramount: 300 mm penetration today is less than half that projected during the planning stages, which has resulted in poor ROI; this experience calls into question the reliability of current projections underlying the case for a transition to 450 mm wafers.

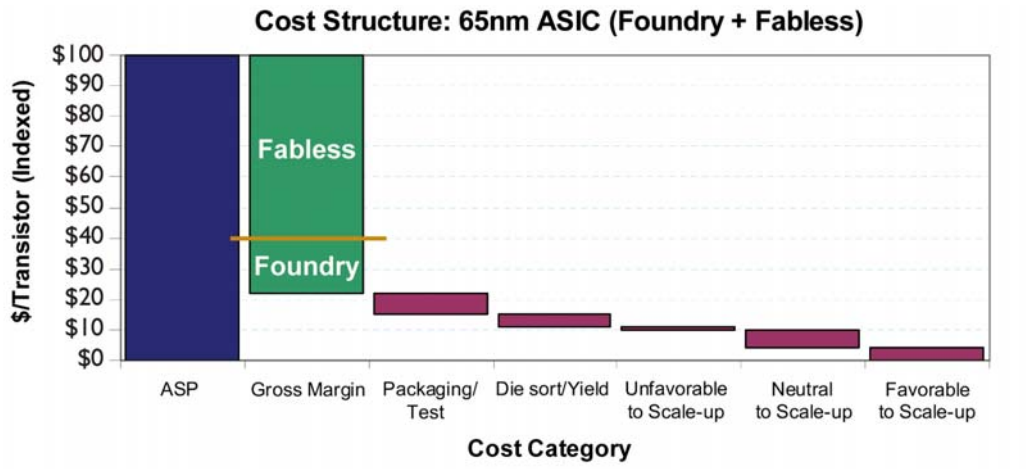
Even more importantly, the economics of the proposed approach to 450 mm could have dramatic negative consequences for the industry. The "savings" of wafer scale-up hinge on ISMI's expectation of cutting capital spend (per equivalent device output) by 45% to 50%, which would translate to an equipment industry ultimately 45 to 50% smaller; the equipment industry would thus take at least a decade (or more) to reach (in real terms) its size prior to the start of the 450 mm transition. In other words, the equipment suppliers would endure (another) decade or more of zero to negative real growth. It is certain that such an industry would have to severely curtail its technical investment, which would undermine the overall ecosystem.

Figure 24 **Scale-Up Provides Hardly Any Benefit to Customer Economics: MPU**



Sources: IC Knowledge cost model, EPWG Analysis

Figure 25 **Scale-Up Provides Hardly Any Benefit to Customer Economics: Logic**

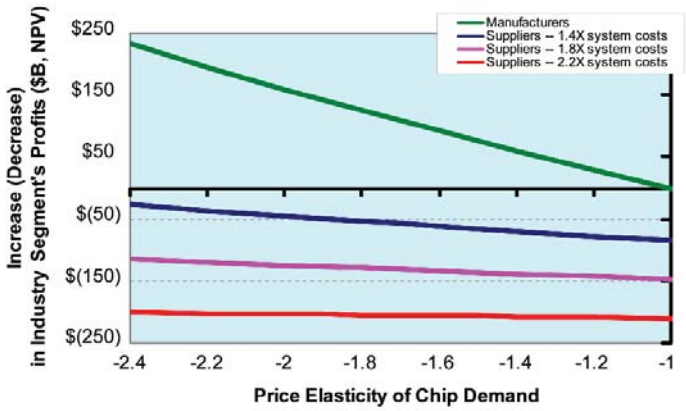


Note: Excludes reticle costs (included in fabless company's RD&E?)

Sources: IC Knowledge cost model, EPWG Analysis

Perhaps most fundamentally, higher-mix demand for chips likely renders larger wafers impractical. A 450 mm transition would undermine the semiconductor industry's ability to meet end-user requirements for fast-cycle-time delivery. While demand to quick-cycle-time production is increasing, 450 mm could introduce a significant cycle time penalty, which early estimates put at more than 50% (Figure 27, page 13). This would be a dangerous move away from recognizing and meeting market requirements. As a result, manufacturers will have to operate their fabs at lower utilization in order to realize acceptable cycle times, thereby eroding and eliminating any conceivable cost advantage provided by 450 mm.

Figure 26 **Wealth Transfer at any Speed**



Sources: IC Knowledge cost model, EPWG Analysis

Table 27 **450mm Cycle Time Scaling**

	300 mm	Longer Time per Wafer	More Wafers per Hour	450 mm
Beam	45%	2.31	1.3	0.80 % of baseling productive time
Vacuum/Atmospheric	35%	1.2	1.0	0.42 % of baseling productive time
Handling/Transport	20%	1.1	1.0	0.22 % of baseling productive time
Total Productive Time	**1**			**1.44**
X-Ratio	3	1.07	1	3.21 Scale-up is roughly similar to a move from 25- to 56-300 mm wafer lot. Impact approximated by analyzing trend across simulations for 25-, 12-, and 6-wafer lots
Total Cycle Time	**3**			**4.62**
Wafer Cycle Time Impact			**1.54**	

Assuming 25-wafer lot

CONCLUSIONS

Evaluating investments involves looking at costs, benefits, investment, and risks. Using a simplified model in which all 450 mm tools have the same wafer throughput as existing 300 mm tools and cost a uniform 30% more while material costs increase only this same mythical 30% overstates the attractiveness of a wafer scale-up by:

- Understating the costs (looking often only at capital costs for greenfield 450 mm fabs)
- Overstating the benefits (by bundling the direct, negligible impact of a pure scale-up with the truly unrelated impact of automation, new fab architecture, tool innovation/CIP, etc.)
- Underestimating the total investment required to reach volume production
- Ignoring the inherent risks.

EPWG has used a fact based cost model to determine the effects of the transition to 450 mm wafers by:

- Evaluating all costs (analyzing total chip costs and how much they would be affected by scale-up; considering total economic impact to the industry—including suppliers and non-users of 450 mm)
- Isolating the direct benefit of scale-up from those that are merely coincidental
- Capturing total investment requirements
- Highlighting the tremendous risks of a transition (risks that all of us vividly remember from the 300 mm transition).

Based on this analysis, it is clear that the industry as a whole would not benefit from 450 mm for the foreseeable future; semiconductor companies would not be economically able to pursue a scale-up in wafer size even if they were technically able to build their own equipment and make their own wafers (vertically integrated).

Given the constraints on development resources, the industry should instead drive fab productivity in higher-impact areas. Specifically, 300 mm Prime represents a set of high-leverage opportunities to create step-change improvements in 300 mm fab productivity consistent with the changing fab environment and the consumer driven market. If the semiconductor industry focuses our combined resources on these initiatives—and continues its unrelenting commitment to pushing process technology forward—we can continue to drive fab productivity for many years to come without resorting to a low-benefit, high-cost, high-risk wafer scale-up.