

300mm Prime: Maximizing the Return on Fab Investment

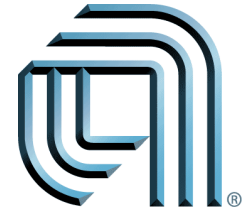
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Foundation Engineering Group*

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Taipei, Taiwan

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think it. apply it.™

Safe Harbor Statement

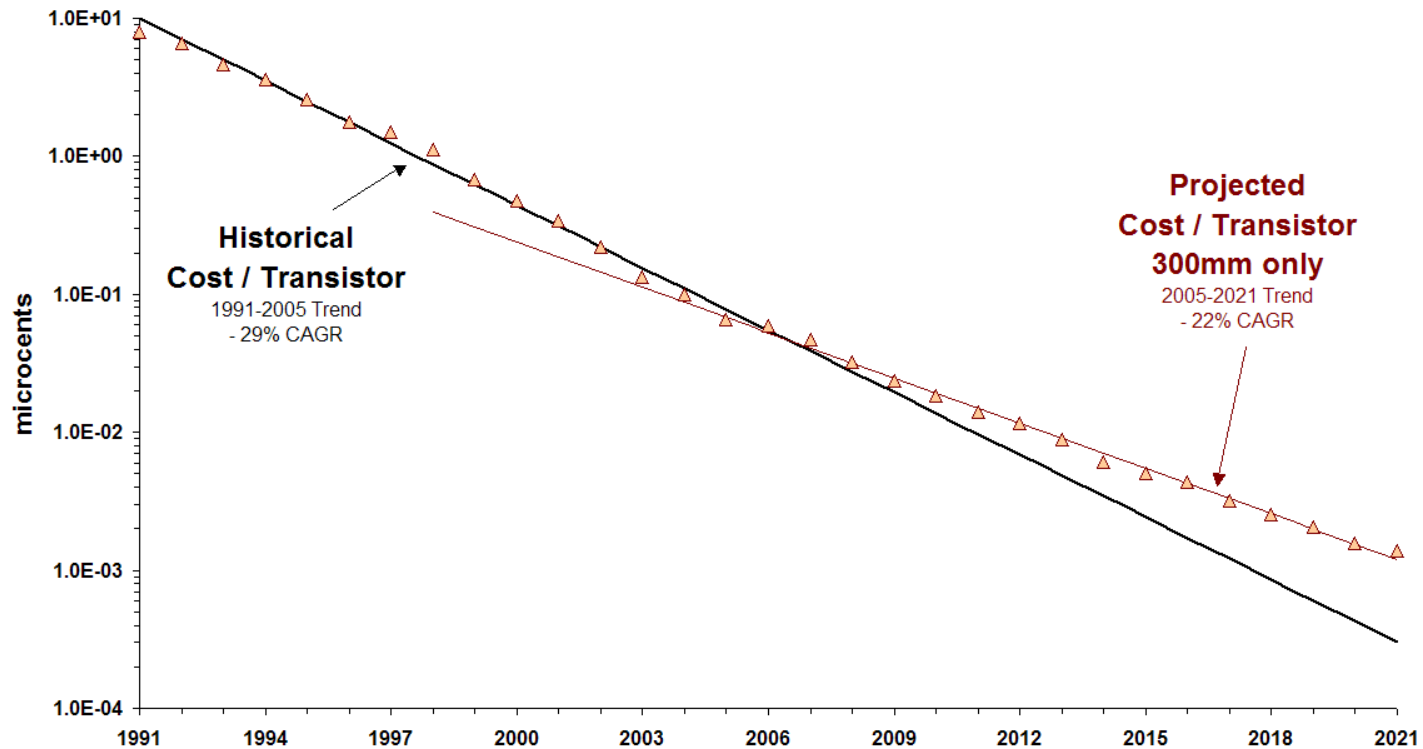


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The “Productivity” Challenge

Average Fab Costs per Transistor

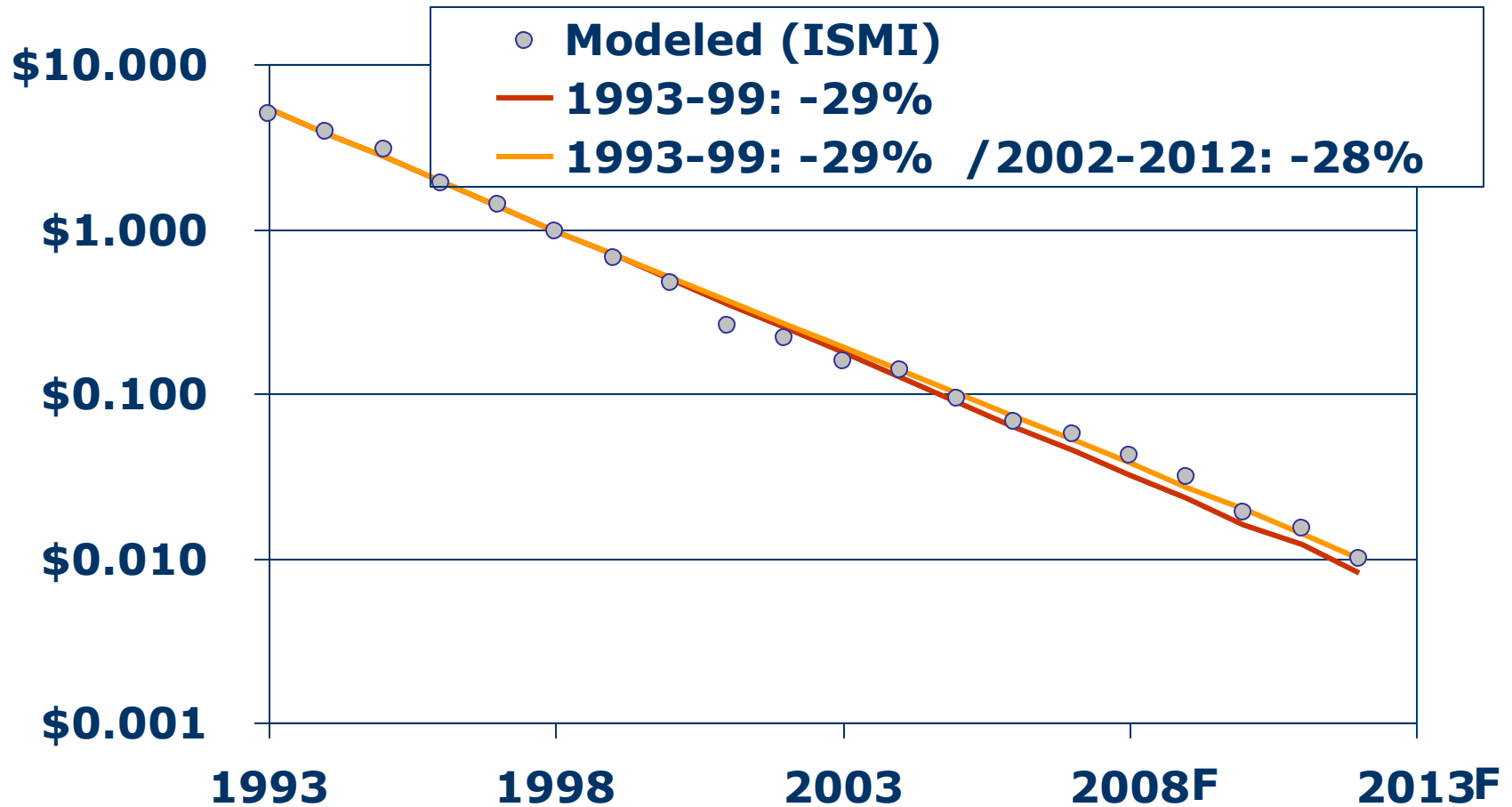


Source: ISMI



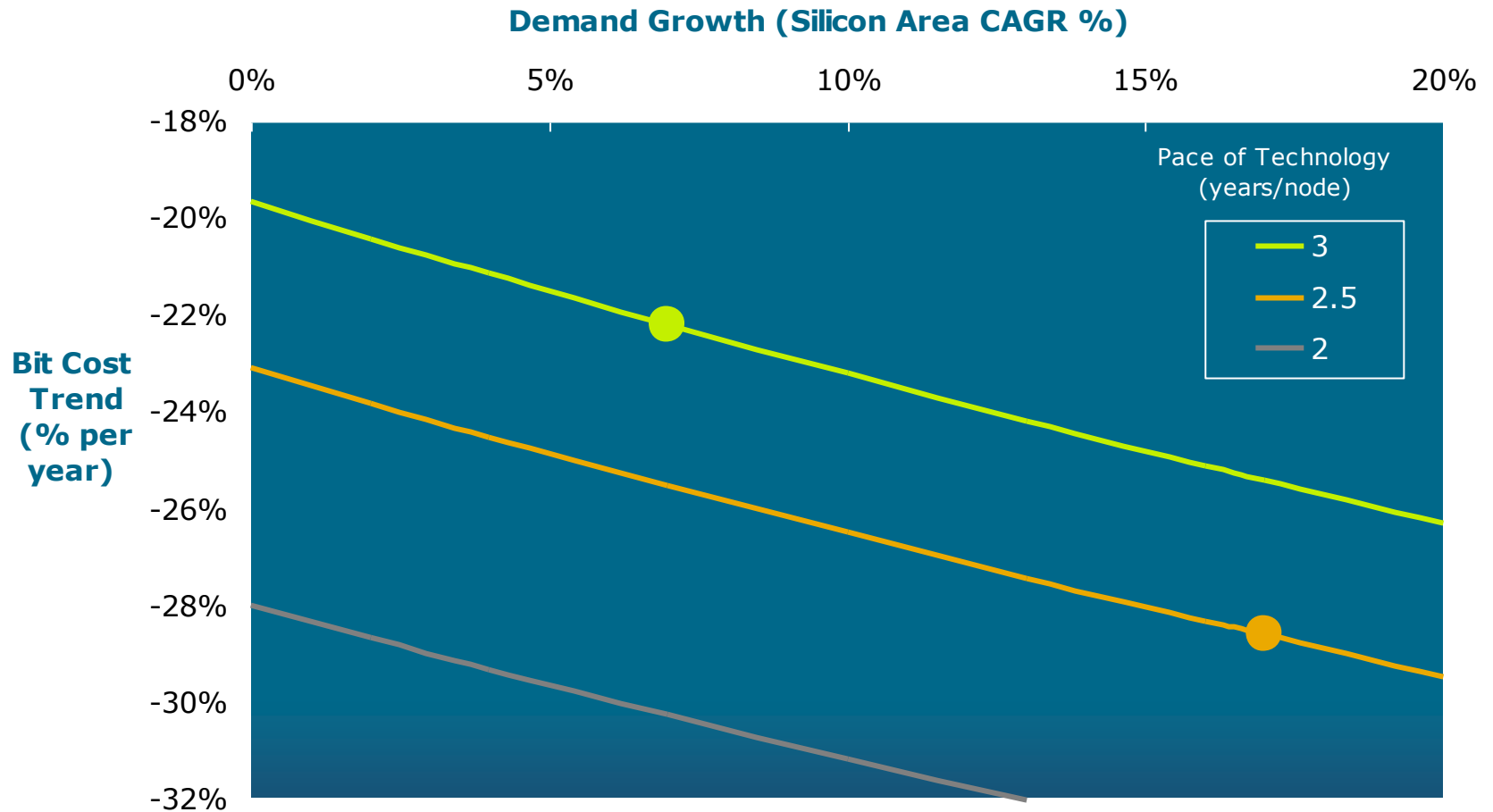
The Challenge... Revisited

Average Fab Costs ($\mu\text{-}\phi$ /transistor)



Source: Applied analysis of ISMI's Economic Model

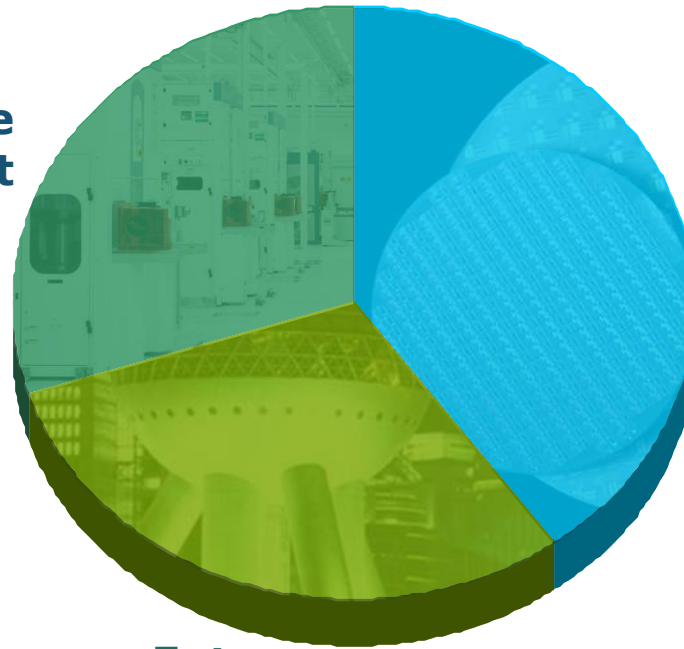
What Are The Root Causes?





How Should The Industry Spend Development \$?

**Installed Base
Improvement**



Next Wafer Size

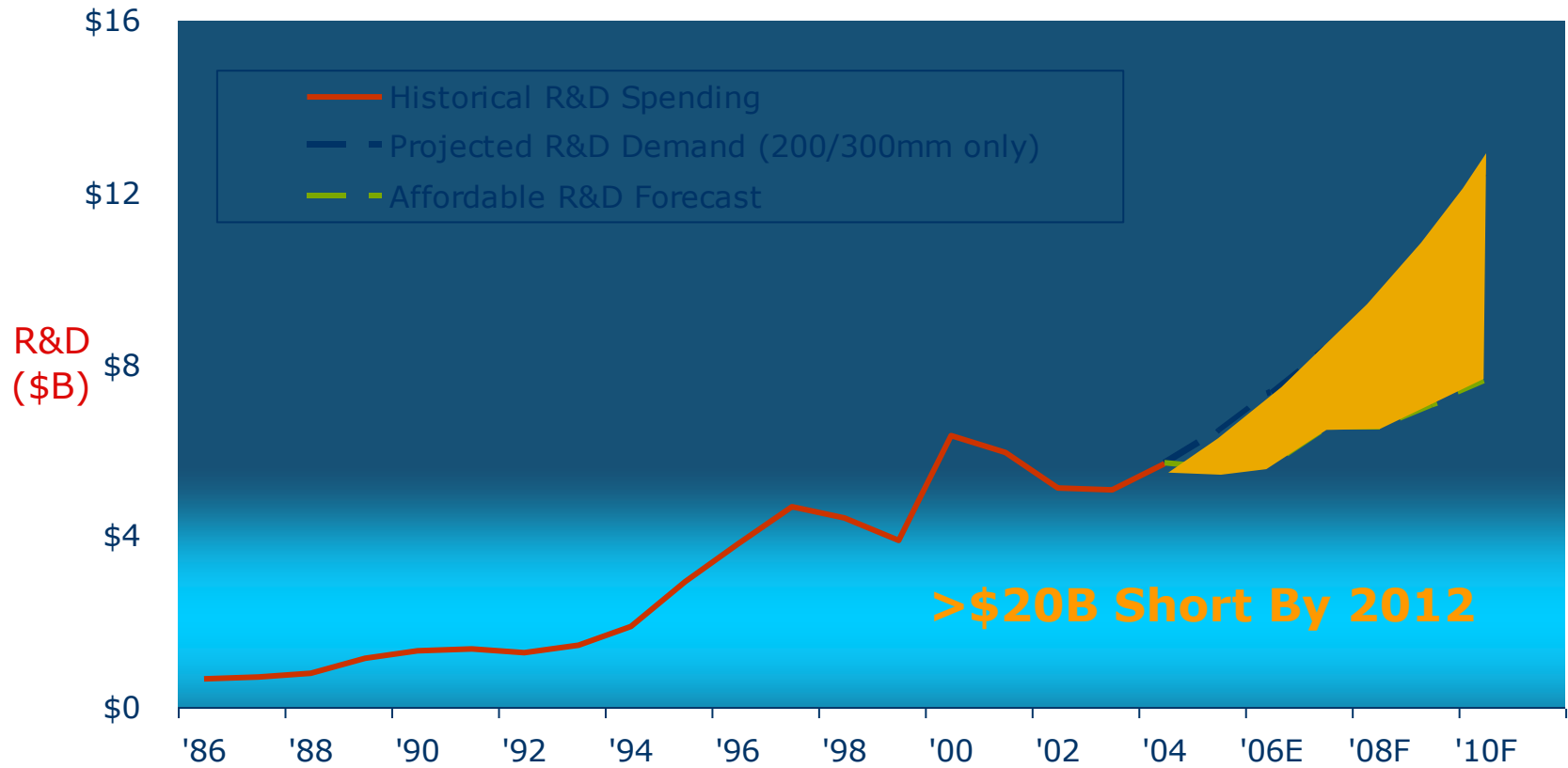
**Future
Technology**

What Should Be The Priorities?

Illustrative



Equipment R&D Gap



Note: Affordable R/D forecast assumes 14% of equipment industry revenues
Sources: S&P, SIA, SEMI, Infrastructure Advisors

Future Technology or Future Substrate?

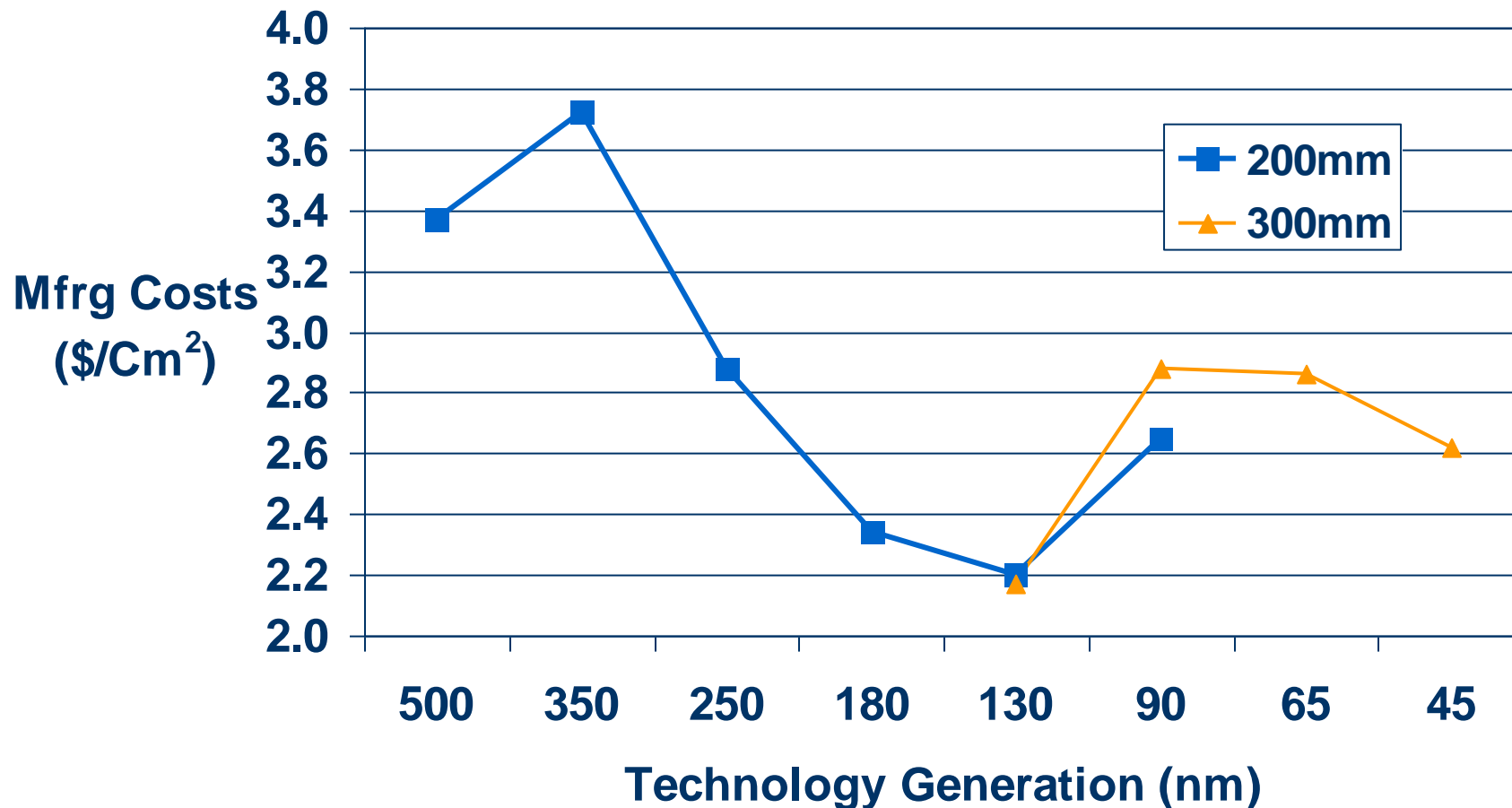


	Technology	Substrate
Value Proposition	<ul style="list-style-type: none"> Double chip performance Increase devices per wafer by 100% 	<ul style="list-style-type: none"> Increase devices per wafer by 125%
Chip Demand/ASP Impact	<ul style="list-style-type: none"> Vital 	<ul style="list-style-type: none"> None
Capital Cost Impact	<ul style="list-style-type: none"> Moderate increase 	<ul style="list-style-type: none"> Significant increase in intrinsic costs for all tools Higher device throughput for some
Variable Cost Impact	<ul style="list-style-type: none"> Moderate increase 	<ul style="list-style-type: none"> Significant increase
Scope of Fab Impact	<ul style="list-style-type: none"> Partial 	<ul style="list-style-type: none"> Total / systemic
Installed Base Benefit	<ul style="list-style-type: none"> Significant 	<ul style="list-style-type: none"> None
Implementation/ Timing Risk	<ul style="list-style-type: none"> Significant 	<ul style="list-style-type: none"> Enormous
Investment	<ul style="list-style-type: none"> Big 	<ul style="list-style-type: none"> Huge

Economic Impact of Wafer Size Transition



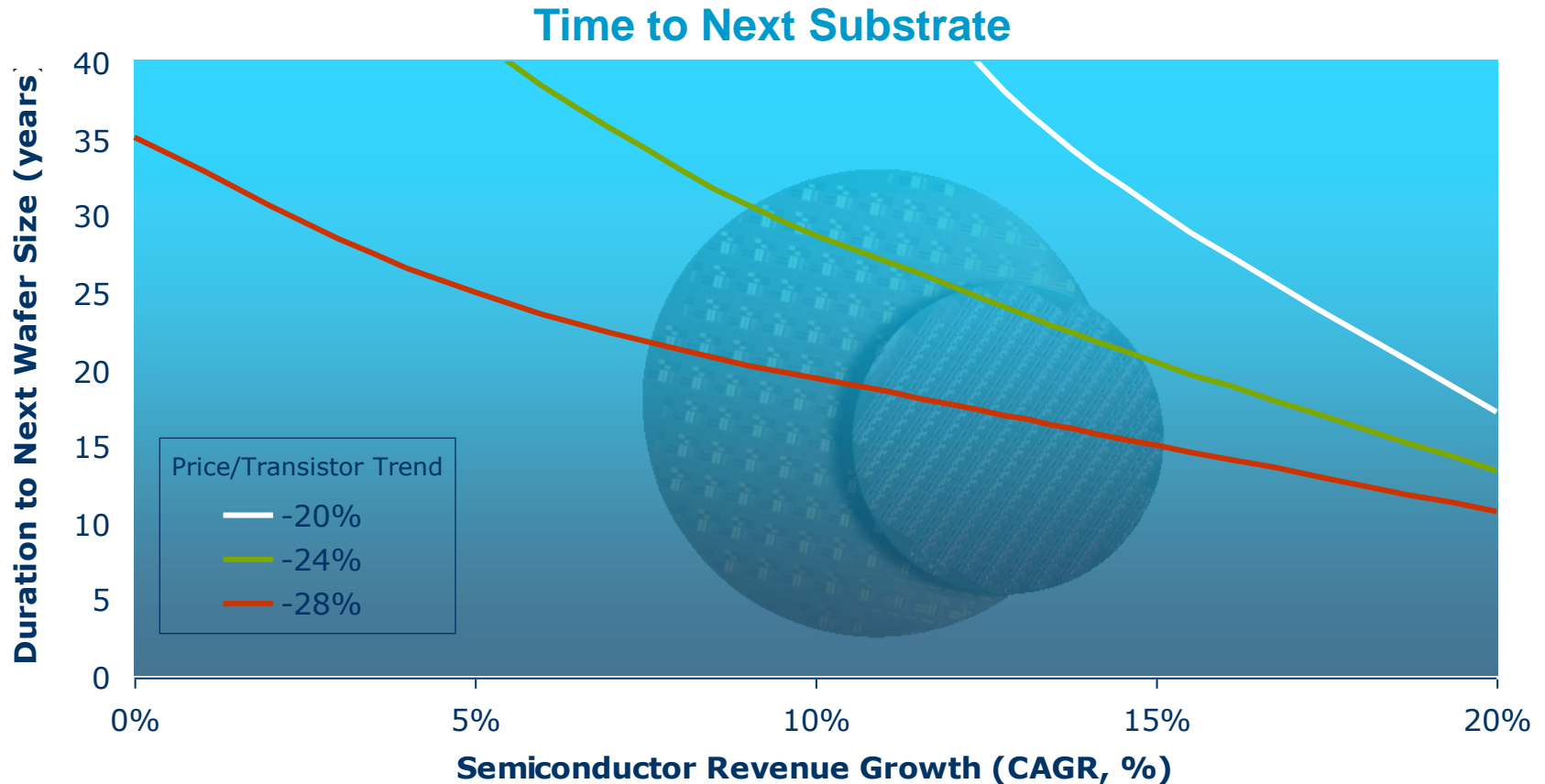
Manufacturing Cost Trend



Note: Year 3 of production, Leading Edge Memory

Source: Applied analysis of ISMI's Economic Model

Demand Drives Wafer Size Life Cycle

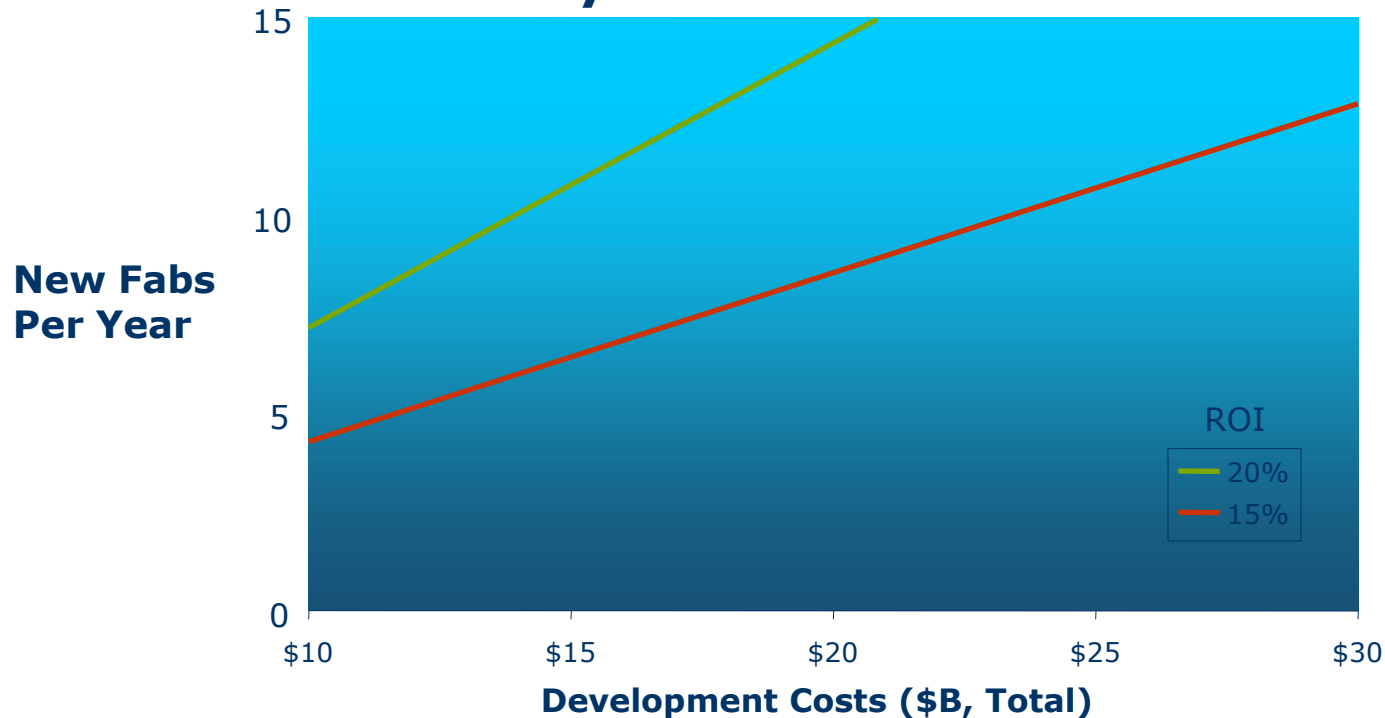


Assumptions: 450mm substrate; 3-year technology nodes; objective is to maintain constant number of fabs

Broad-Based Adoption Required to Justify 450mm Investment



New 450mm Fabs Required to Pay Back R&D Investment

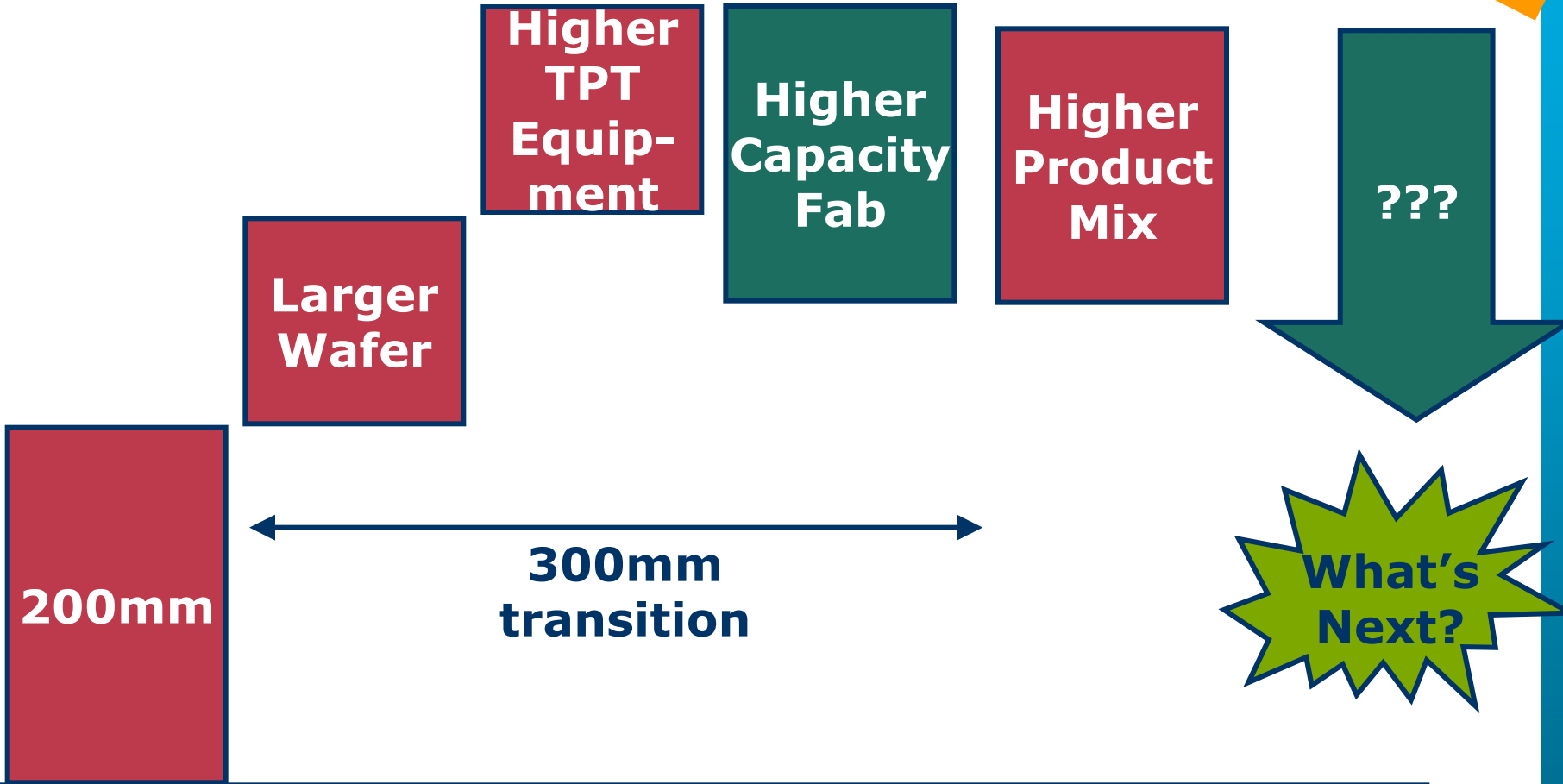


Note: Entire food chain modeled as a single entity earning back return on development funds through manufacturing cost savings; this investment may not be sufficient to allow suppliers to recoup investment

Managing Variability



Conceptual



Product + Process Variability



Maximizing the Return on Fab Investment

Optimize fab operations



Build foundation of rapid, differentiated, technology solutions

- Extend Litho
- Enable transistor performance
- Scale interconnect RC
- Scale memory density (strain)
- Resolve nano defects

