Cycle Time, Productivity Emerge as Key Issues at ASMC

Cycle Time, Productivity Emerge as Key Issues at ASMC

At the recent Advanced Semiconductor Manufacturing Conference (ASMC) in Stresa, Italy, over 200 attendees learned the latest tools, techniques and processes for advanced chip making—from over 80 technical papers. To compete in markets that are increasingly driven by consumer products, a common theme ran through the keynote presentations and in many papers. Namely, there is an overwhelming need for productivity and cycle-time improvements.

Semiconductor device markets are increasingly consumer-driven. In fact, 2007 marks the first time that chips from consumer markets outpaced industrial and business markets. In addition to intense pricing pressure, this also means that product variety is on the increase and product life cycles are becoming shorter. These trends impact semiconductor fabs because of the critical need to address many more products in smaller lots with dramatically reduced manufacturing cycle times. A fab that can produce many products with short cycle times is an “agile fab.” It’s also a fab that is fast-to-market, which translates into the higher advanced selling prices (ASPs) at the inception (and throughout the duration) of the product life cycle.

At SEMICON West, a panel of experts will also explore this topic in a panel discussion entitled. “Next Generation Fab: Defining 300 mm Prime” on Thursday, July 19 from 8:30am –10:00am at Moscone Center, Esplanade Hall.

Priority Number One

According to the opening ASMC keynote, short-cycle time manufacturing is the key to success. Areih Lev Greenberg, senior principal at Qimonda AG (Germany), states that “Priority number one in the industry has to be reducing cycle time.” He stresses that cycle time rules, because it leads to faster new product introduction, product delivery to customers, and time to money. In addition, he says that it mitigates both risk by reducing ASPs and the impact of excursions due to faster response.

“New technologies lead to an increased number of litho mask layers and degradation of factory cycle time,” according to Greenberg, so breakthrough approaches to continuously reduce cycle time are required. He sees the future with simpler, smaller tools replacing the inherently complicated tools. He also believes that reduced tool setup times and standard lot size changes will make a big difference.

Greenberg also stated that that “300 mm Prime is an evolutionary approach to identifying and implementing 300 mm productivity improvements that are scalable to the next wafer size manufacturing.”

At ASMC, Greenberg wasn’t alone in his thoughts on 300 mm Prime. Another keynote speaker, Iddo Hadar, CTO of Foundation Engineering at Applied Materials (California), shared his views on 300 mm Prime. He emphasized that the three most important goals of the initiative are to:

- Reduce losses between tool and fab throughput;
- Reduce fab resource use (power, water, etc.); and
- Reduce wafer “waiting time” due to batching.

Hadar encouraged companies to differentiate themselves by pursuing “revolutionary changes,” moving to small lot manufacturing, and like Greenberg, urged a focus on simpler, smarter tools.

ASMC: A Forum for Technical Professionals

ASMC 2007 is presented by SEMI and the IEEE. The two-day conference is co-sponsored by the IEEE Electron Devices Society (EDS), the IEEE Components, Packaging and Manufacturing Technology Society (CPMT). Over 80 technical papers were introduced at ASMC on various subjects including: Design for Manufacturability, Advanced **Process** Control, Defect Inspection, FA/FD/300 mm, Lithography, Advanced Processes and Materials, Advanced Metrology, Yield Enhancement, Cost Reduction and Equipment Productivity, Yield Modeling, and Industrial Engineering.

ASMC provides a unique opportunity for technical professionals to learn novel solutions to wafer fab manufacturing issues. Although numerous papers and authors discussed the issues of productivity and efficiency in the fab, three research results really stood out.

Agility through Range Management

One way to improve fab agility was through a **Range Management** System. This paper described how IBM’s 300 mm fab in New York processes a mix of low and high volume production technologies in conjunction with processing development hardware for future technologies. According to Sameer T. Shikalgar, **range** analyst in the fab and author of a research paper presented at ASMC, “**Range Management** is a **methodology** for **managing daily work flow** in a fab **incorporating LEAN management concepts**.” This involved mapping **process** routes, setting **daily** throughput targets based on WIP and capacity, and modifying the dispatch rules to achieve the targets for each **range**.

Shikalgar stated that one of the keys to success involved the dispatching of monitor wafers, which is usually a manual operation. With the **Range Management** system, the routes for the monitor wafers are integrated in the system and are dispatched along with product wafers. Since the releases of the monitor wafers are also controlled like product wafers, it eliminates the

need for manual intervention. The results speak for themselves. Shikalgar states that the "**Range Management** system resulted in closed lot cycle time being reduced by 33% and the distribution of cycle time by 2.5 times" and that the data indicates that "the reduced cycle time has greatly improved productivity and yield learning."

Reducing Cycle Time with Small Batch Size

Another way to definitely reduce cycle time is focusing on the "move batch size," also called the "transport lot size." Using conventional 300 mm factory architecture with batch tools, Daniel Babbs and Robert Gaskins from Brooks Automation (Massachusetts) presented a paper describing factory simulations that illustrate the relationship between transport lot size and the overall cycle time. Cycle time is defined "as the elapsed time from when a lot is released at the start of the **process** flow to when the lot has been processed at the last step in the **process** flow." In other words, cycle time includes the actual wafer processing time plus all the "waiting time" due to tools (utilization, setup, or repair).

The Winning Scenario Was …

According to Babbs and Gaskins, using the 25 wafer lot as the baseline and comparing all scenarios with 50 products, the five-wafer lot reduced average cycle time the most—by 13.7%. In addition, "this same five-wafer lot scenario with a 75% reduction in **process** tool setup time reduced the average cycle time by 24.5% from the baseline." They have several other interesting findings, including results on setup time, first-wafer delay, and implications for factory stability.

Improving Priority Lot Cycle Times

Kilian Schmidt from AMD Saxony described how challenging it was to combine reduced lots and reduced cycle times and achieving both objectives required a"holistic approach." AMD experimented with the 300 mm Prime goals and priority lots and found that while only a small portion of WIP is priority lots, their positive results stand up to scrutiny.

Schmidt demonstrated how "substantial cycle time benefits for super-hot and hot lots can be achieved with a single wafer toolset and smaller lot size. These benefits can easily reach the 50 percent CT (cycle time) reduction **range**." He showed how the size of some hot lot cycle time components is "driven by normal lot size while others depend on hot lot size only." In addition, the research showed that a new system of interrupting current jobs in **process** to save costs associated with priority lot cycle time may be feasible.

300 mm Prime at SEMICON West

At SEMICON West, please plan to attend a panel of experts discussing "Next Generation Fab: Defining 300 mm Prime" on Thursday, July 19 from 8:30am–10:00am at Moscone Center, Esplanade Hall.

ASMC 2008—Boston

Next year, the ASMC 2008 will be in **Boston**, Massachusetts. Once again, technical professionals from all over the globe will convene to debate and present the issues. Be there!

For More Information on ASMC

Please visit www.semi.org or email Margaret Kindling at mkindling@semi.org.