Economic Challenges and Opportunities in the 300 mm Transition

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With development risk fully borne by the equipment industry and a two-year delay in the main deployment of 300 mm equipment, the wafer size transition runs the risk of allowing low or non-existent return on investment for semiconductor equipment manufacturers if a cost ratio of 1.3X the cost of 200 mm equipment must be realized. As a result, the equipment industry may have insufficient capital needed to invest in <0.15 µm technology, advanced materials and processes and the eventual transition to 450 mm wafers. Higher tool cost multipliers are clearly affordable. For example, a 300 mm fab producing 256 Mb DRAMs could offer an incremental profit margin of $3.6-$1.3/cm^2 with a multiplier in the 1.4-2.0 range. Therefore, there is an excellent opportunity for win-win situations.

300 mm Challenges

1. Concentrated risk

A key problem burdening the industry's equipment supplier/device manufacturer interdependence is continuous shifting of responsibility for technical advances to key equipment suppliers[1]. In past wafer size transitions, customers shared risk and development costs with equipment manufacturers, along with development of key technologies at Bell Labs, NTT and IBM's T.J. Watson Research Labs. In the 200 to 300 mm transition however, semiconductor manufacturers dedicate R&D dollars almost exclusively to IC design, process integration, yield enhancement, etc., leaving the bulk of the 300 mm R&D burden to equipment manufacturers.

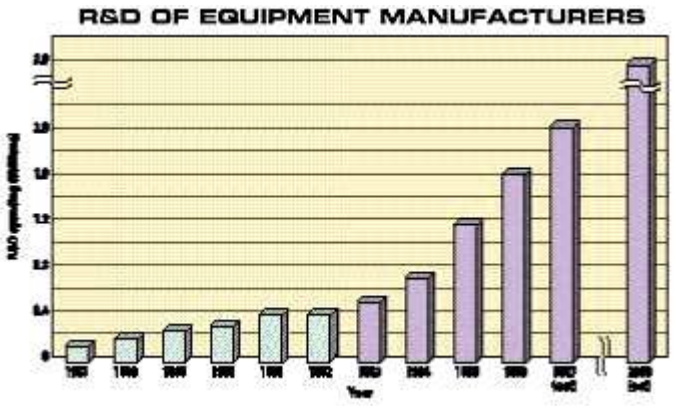

Fig. 2. Equipment industry R&D spending has surged by 30%/year from 1993 to 1997. (Source: Equipment industry annual financial reports, VLSI Research, DataQuest, others)

2. Technical barriers

The 200/300 mm transition is not simply a scaling effort; it involves fundamental technology shifts. For logic ICs, these include:

- Copper-based interconnects instead of traditional aluminum alloys,
- Low-k (<3.0) and ultra-low-k(<2.6) interlevel dielectrics,
- Low-resistivity contact materials: Ni or Co instead of Ti,
- Low-resistivity gate materials,
- Gate oxides below 40 Å with diffusion barriers and
- Shallow junctions with raised sources and drains.

For DRAM devices, the changes include:

- New storage capacitor materials: tantalum pentoxide (Ta_2O_5), barium strontium titanate (BST) and platinum zirconium titanate (PZT);
- New electrode materials: platinum, HSG and TiN;
- Vertical stack or very high aspect ratio trench capacitors and
- High aspect ratio (. 10:1) contacts.

Another critical issue is the immaturity of optical lithography's calcium fluoride lenses for argon fluoride laser (193 nm) exposure. Further, high IC manufacturing yields (with aggressive device scaling) demand high precision and high throughput metrology.

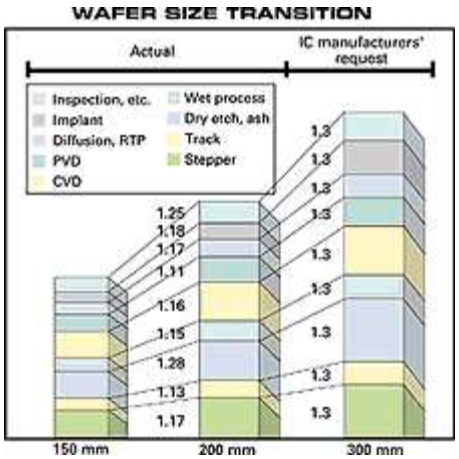

Fig. 3. ASP multipliers for 150 to 200 mm (actual) and 200 to 300 mm, as requested by IC manufacturers.

3. Transition timing uncertainty

Originally, the 300 mm wafer transition was expected to occur coincidentally with 0.25 or 0.18 µm processes. It now appears that DRAM ICs will have device dimensions in the 0.18 to 0.15 µm range, while logic devices will be in the 0.15 to 0.13 µm range. Several factors are affecting the timing of this transition, including:

- Continued focus on rapid critical dimension shrinkage with 200 mm technology, therefore a need to develop ne

  w technologies simultaneously for 200 and 300 mm equipment;
- Lack of 300 mm equipment with comparable maturity to that of 200 mm equipment (especially unavailability of lithography tools with wafer throughput <80 wafers per hour;
- 200 mm IC production over capacity;
- Economic problems in Asia and
- IC pricing impact of the sub-$1000 personal computer.

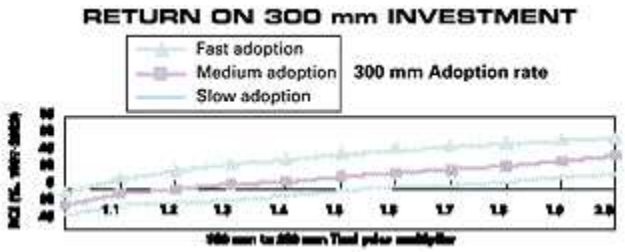

Fig. 4. ROI through 2003 as a function of the 300/200 mm tool ASP multiplier and rate of adoption: 22% by 2003 (medium rate), one-year delay or one-year acceleration.

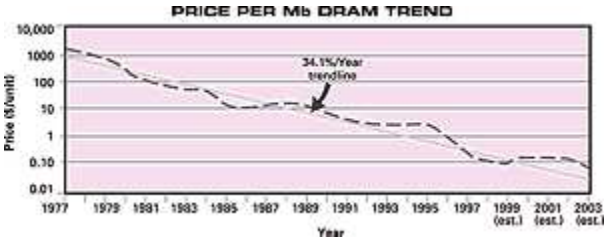

Fig. 5. DRAM price trend indicates a 256 Mb DRAM will sell for $25-$30 in 2001 (about 10 cents per Mb).

As a result, the bulk of 300 mm pilot lines will start taking equipment deliveries by the first and second quarters of 2000, a full two-year delay, as compared to the July 1997 forecasts (Fig. 1), with operational capabilities three to six months later and mass production beginning in the first half of 2002.

Implications

Total R&D spending by the wafer fab equipment industry increased by over 30% per year from 1993 to 1997 and could reach $3.6 billion per by 2000 (Fig. 2). Of course, the only means of funding such investment is via the revenue generated by tool sales. In the transition from 150 to 200 mm, the equipment average selling price (ASP) multiplier averaged 1.18, with virtually no changes in manufacturing materials or structures (Fig. 3). For the shift to 300 mm, IC manufacturers are requesting a multiplier of 1.3 or less[2]. Given the stated requirements for 300 mm technology, the equipment

industry's investment in 300 mm equipment development and commercialization from 1996 through 2001 could exceed current estimates of $4.3 billion easily.

The return on this investment (ROI) would be less than 5%, assuming 300 mm technology becomes 22% of the equipment market by 2003[3]. If that level of penetration takes an additional year to materialize (as current pilot/manufacturing timelines indicate), even a 1.55 ASP multiplier results in zero ROI by 2003; a 1.3 multiplier would yield ROI in the negative two-digit range (Fig. 4).

In addition, the 1.3X price multiplier will inhibit the equipment industry's ability to provide timely, advanced technology manufacturing equipment with necessary scaling beyond 0.15 µm. R&D funding for the 300/450 mm transition, expected by SEMATECH to begin in 2008, will be scarce also. Finally, slim 300 mm profits may force further consolidation among equipment suppliers.

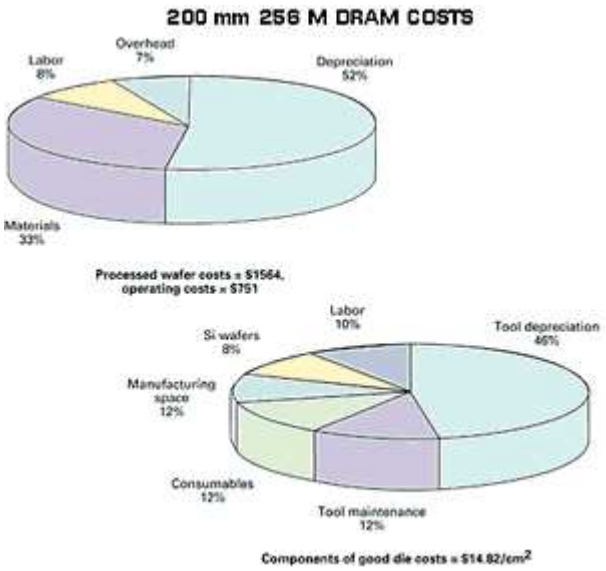

Fig. 6. Each 200 mm wafer costs about $1600 to manufacture, while each good 256 Mb die costs about $15 per cm² (calculation based on fundamental analysis of IC manufacturing investment and processing costs).

300 mm Win-win opportunities

So, is 300 mm a bad deal? Not at all. A realistic examination of risks and rewards indicates an opportunity for a "win-win" scenario for both semiconductor IC manufacturing and equipment industries. In it, the equipment industry earns profits it needs to advance state of the art and manage new investments, while semiconductor manufacturers benefit from lower production costs to earn a substantial return.

The economic factors driving larger wafer transitions are straightforward. A greater number of dice per wafer allows greater production of ICs, assuming the same wafer throughput. If costs increase by x%, and the number of ICs increases by y%, and y >x, cost per die decreases (by 100%-(100%-x)/(100%-y), to be precise).

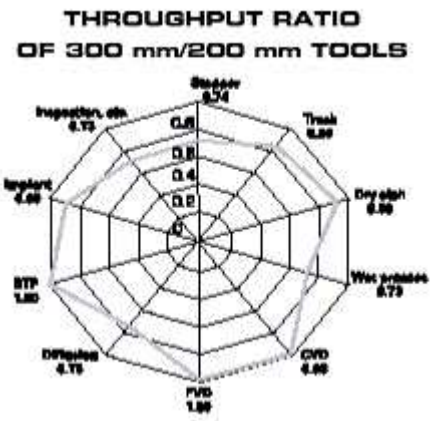

Fig. 7. Estimated throughput for 300 mm equipment relative to its 200 mm counterpart, based on industry -wide analysis and subject to limitations of scan speed and batch size.

Since DRAM devices suffer from the highest price erosion and therefore pose the highest manufacturing cost pressure, we considered a 256 Mb DRAM fab using 0.18 µm design rules in our analysis[4]. ASP of a 256 Mb DRAM in (early) 2001 is estimated to be $25-$30, based on extrapolation of current 16 and 64 Mb DRAM price trends (Fig. 5). If we assume a die size of 100-120 mm^2, the ASP per unit area is $25/cm^2 on 200 mm wafers. These 2001 estimates are consistent with expected volumes and technology maturity.*

Volume manufacturing cost of 256 Mb DRAMs on 200 mm wafers would be nearly $1600/wafer, or a good die cost of close to $15/cm^2 (Fig. 6) and a margin of about $10/cm^2. Tool depreciation and maintenance account for over half of the total cost. Key yield assumptions and tool throughput

numbers for the 200 mm baseline fab and its 300 mm equivalent are shown in Table 1 and Figure 7, respectively. We assumed lower line yield (91% vs. 92%) and probe yield (86% vs. 89%) for the first generation of 300 mm fabs vs. 200 mm.

The number of dice per wafer provided by 300 mm relative to 200 mm wafers is 2.35X. The transition potentially benefits DRAM manufacturers via lower fab depreciation and maintenance costs (Fig.8). Based on this fundamental data, this analysis indicates that at the extreme case (if 300 mm tool prices are identical to 200 mm tool prices, ie., multiplier of 1.0), the DRAM manufacturer could obtain an incremental value, or additional margin, of about $5/cm^2. However, this tool cost multiplier of 1.0 would reduce the margin of the semiconductor equipment industry by over 55%, limiting its ability to invest in R&D for sub-0.15 µm technology.

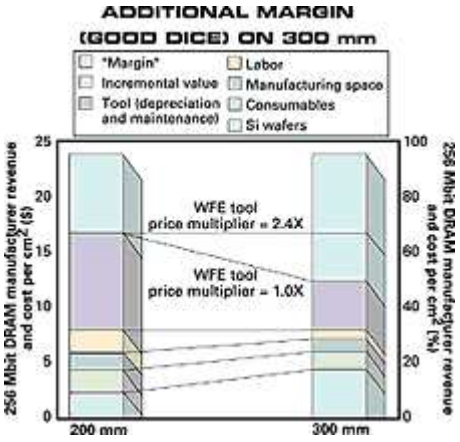

Fig. 8. When comparing production of DRAMs on 200 vs. 300 mm wafers, the DRAM producer gains incremental value - additional margin of good die per square centimeter - right up to a 300/200 mm price multiple of 2.4.

Instead, incremental revenue for the 256 Mb DRAM case can be distributed between IC manufacturers and the equipment industry in a way that results in a competitive equipment industry, capable of meeting industry demands, including a reduction of manufacturing cost per die. The data from Figure 8 indicate that a 300 mm tool price multiplier in the 1.4-2.0 range would give a manufacturer of 256 Mb DRAMs an incremental value in the $3.6-$1.3/cm^2 range respectively, enabling a win-win scenario for both industries (Table 2).

Table 1.
256 Mbit DRAM: 200 vs. 300 mm

Design rule	micron	0.18	0.18
Wafer size	mm	200	300
Wafer area	mm^2	31,419	70,683
Die size	mm^2	120	120
Gross die per wafer	pcs	223	548
Probe yield	%	89	86
Line yield	%	92	91
Wafer starts	Wafers/wk	6000	6000
Wafer outs	Wafers/wk	5520	5460
Utilization	%	92	92
Good die per wafer	pcs	198	471
Wafer cost	$	100	600
IC revenue	$/cm^2	25	25
Obtainable chip ratio		1.00	2.35

Summary

The 200 to 300 mm wafer size transition is occurring coincidentally with significant device technology, processing and materials changes. In addition, semiconductor industry behavior in sponsorship, leadership and risk-taking has changed. No longer is one IC company willing to lead the effort. The industry carries the bulk of the investment burden (an estimated investment of $4.3 billion from 1996 to 2001). This risk is exacerbated further by the IC industry's expectation for a 300 mm tool price of <1.3X the 200 mm tool price and delays in starting pilot manufacturing lines. The return on the equipment industry's investment is at risk of being below 5% by 2003, limiting its ability to invest in R&D and technology commercialization beyond 0.15 µm.

A win-win situation for both the IC manufacturing and equipment industries can be achieved for 300 mm tool price multipliers in the 1.4-2.0 range. Semiconductor manufacturers that quickly seize the 300 mm opportunity will boost financial returns significantly while ensuring long-term availability of key suppliers of process technology.

*However, 256 Mb DRAM pricing and timing could change due to emergence of the 128 Mb DRAM and possible changes in device demand. The revenue value for logic, especially for microprocessors, is even higher.

Table 2. Model Results

	200 mm	300 mm
Area factor	1.0	2.35
IC manufacturers' cost factor target	1.0	1.30

Equipment cost factor forecast	1.0	1.4-2.0
IC manufacturers' incremental value ($/cm^2)	--	3.6-1.3

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